Characterisation of the new tracker sensors for the CMS experiment at CERN

As part of the phase-2 upgrade of the CMS detector, towards the high-luminosity phase of the LHC

Ali Safa

Master thesis submitted under the supervision of
Prof. Dr. Ir. Frédéric Robert

the co-supervision of
Prof. Dr. Ir. Pascal Vanlaer

in order to be awarded the Degree of
Master of Science in Electrical Engineering

Academic year
2019 – 2020

Title: Characterisation of the new tracker sensors for the CMS experiment at CERN

Author: Ali Safa
Master of Science in Electrical Engineering
Academic year: 2019 – 2020

Abstract

I-V and C-V curves are crucial measurements required to characterise Silicon sensors. They must be performed at reception and at several steps of particle detector module assembly to spot potential damages. High-voltage (1kV) biasing of those sensors and accurate current measurements (50μA max) are mandatory for sensor characterization. High-voltage electrometers and LCR meters with proper decoupling are the typical instruments used to perform those measurements. Those instruments are rather expensive (10k euros range) and are often over-specified for this precise task. We developed a system tailored to perform both I-V and C-V measurements of sensors in one compact, low-cost instrument. The instrument is built around a PCB that implements a low ripple (100mV) 1kV high-voltage power supply, a high-side AC/DC current measurement circuit and a capacitance measurement circuit. The instrument is coupled to an external signal generator, a computer that extracts electrical parameters and the I-V/C-V curves, and a Programmable System-On-Chip (PSOC) which handles source control in addition to current, voltage and voltage/current phase measurements. On top of that, temperature and relative humidity are monitored. Finally, low-voltage DC regulators can power readout electronics of fully assembled modules to provide a standalone test station usable in sensor/module characterisation or in thermal cycling.

Keywords: Silicon sensor, particle detection, embedded system design.

Preface

My collaboration with the *Inter-university Institute for High Energies* started way before this master thesis project, in Summer 2017, when Prof. Robert and Prof. De Lentdecker gave me the opportunity to join the institution as part of a research grant program for students in engineering (so-called *BIR* grant). They opened me the doors to the passionate world of the CMS detector which became an endless source of knowledge and insights in electronics design, not only during this Summer internship but also during the MA1 project and the master thesis. During this master thesis, I had the chance to collaborate in a daily basis with Prof. Vanlaer and Dr. Allard. Their valuable advice allowed us to produce fast results which in turn, enabled me to present my work during an international workshop on particle detectors in Vienna (TREDI 2020 "Trento" Workshop). I felt blessed to already receive such opportunity as a master student. My personal goal was to span a broad spectrum of electronics engineering during this project, from circuit design to firmware, software and signal processing. I hope that reading this thesis will be a testimony to my passion for electronics.

Acknowledgements

First of all, I would like to express my gratitude towards my supervisors Prof. Frédéric Robert, Prof. Pascal Vanlaer, Prof. Gilles De Lentdecker and Dr. Yannick Allard for their continuous support and excellent advice throughout this project. I would also like to thank the whole IIHE team for their friendliness and support during my stay at the institution.

"The sea was calm, and glittered under limitless sky - it was going to be a wonderful morning, the sort of restful brilliance you get, the sky exhausted of clouds, after days of storms. The light grew brighter, revealing the day, and it just got better, as this rosy dawn became a sunset in reverse."

P. Theroux, *The Pillars Of Hercules*

Table of Contents

List of Figures

List of Tables

Chapter 1
Introduction

The work presented in this master thesis is part of the upgrade of the Large Hadron Collider (LHC) for CERN.

In order to enhance its performances, the LHC needs an upgrade. This upgrade will lead to the so-called high-luminosity phase of the LHC (HL-LHC) which will allow a finer study of particles such as the Brout-Englert-Higgs boson, enabling the discovery of new phenomena. The HL-LHC is expected to be operating in 2026. As part of this project, the Compact Muon Solenoid (CMS) experiment, one of the four particle detectors located around the LHC, will also undergo a major upgrade to cope with the HL-LHC luminosity. The CMS detector is composed of a plethora of sub-detectors like various particle trackers and calorimeters. This work focuses on the so-called *phase-2 upgrade* of the CMS Silicon tracker.

The Inter-university Institute for High Energies (IIHE, ULB/VUB) is at the epicentre of this upgrade as it is expected to produce more than 2500 Silicon tracker modules. A clean room furnished for that purpose is currently being installed at the IIHE. At the core of this large-scale production, an electronics testing set-up used to characterize and approve each Silicon sensor before mounting them on the modules is strongly needed. Those Silicon sensors are formed by a few thousand P-N junctions in parallel. Thus, this characterization will consist in the identification of the full-depletion voltage of each sensor through the measurement of *leakage current v.s. reverse-bias voltage* and *sensor capacitance v.s. reverse-bias voltage* (so-called I-V and C-V curves).

The design of such testing equipment is subject to numerous constraints. First, the sensor modules will operate at the low temperature of $-35°$C. Consequently the test-stand that will be designed should ideally work at this temperature (reached using an industrial fridge), minimizing the cabling between the outside and the inside of the fridge. Secondly, the design of the testing device is subject to tight time constraints as it needs to be ready when the production of the new modules will be launched next year. Finally, pricing constraints are also present as the instrument should cost no more than a few hundred euros in parts. Due to the nature of the tests that would need to be conducted, high precision measurement circuits operating at high-voltages and low temperatures are needed which makes the design of such low-cost system harder.

The design of an automated silicon sensor testing set-up from the ground-up under the constraints cited above is thus a considerable challenge.

The instrument to design will be composed of a low-voltage power-supply, a high-voltage generator (to reverse-bias the sensors), a current meter, a capacitance meter, temperature sensors and humidity sensors. The targeted specifications are given below.

- **High-Voltage range**: 0 to $\pm$1000V
- **Maximum ripple amplitude**: 100mV
- **Two current measurement ranges:** $\pm 7\mu$A and $\pm 50\mu$A with a precision of $\sim 6n$A and $\sim 30n$A respectively
- **Current measurement sampling rate**: 4kHz
- **Capacitance range**: 1-60nF
- **Capacitance estimation error on whole range**: $< 1\%$
- **Working temperature range of components**: $-35°$C to $65°$C
- **Dimensions**: 30cm $\times$15cm.
- ***Price***: $<$ 300 euro (PCB in Europe $\sim$ 50 euro, components $\sim$ 250 euro).

This thesis aims to present the design and experimental validation of a complete testing system for the Silicon tracker sensors that will be produced at the IIHE. First, the context in which the thesis takes place will be explained. Then, the working principle of the Silicon sensors will be detailed, followed by the high-level description of the complete testing system. After that, the design of the numerous electronic circuits used within the system will be explained. Finally, the experimental validation of the system will be detailed.

Chapter 2
The Large Hadron Collider update project

In this chapter, the context of the project is detailed before emphasizing on the project itself and technical developments.

2.1 The Large Hadron Collider Upgrade Project

The Large Hadron Collider (LHC) is the largest and most powerful particle accelerator in the world [1] which can achieve a centre-of-mass energy of 13TeV. The LHC can accelerate protons and heavy ions and is formed by a 27-km ring of superconductor magnets (needed to generate high magnetic fields) and accelerating equipments used to boost the energy of the particles along the ring. The superconductor magnets are used to guide the two high-energy particle beams traveling in opposite directions in two separated vacuumed tubes at nearly the speed of light before collision. The collisions are made to occur at four different locations around the ring, corresponding to four distinct particle detectors: ALICE, LHCb, ATLAS and CMS.

The LHC agenda is composed of periods of runs, where the accelerator is used to produce collisions and generate data, and long shut-downs (LS), where the accelerator is upgraded to enhance its performances. The calendar from 2015 onward is shown in figure 2.1.

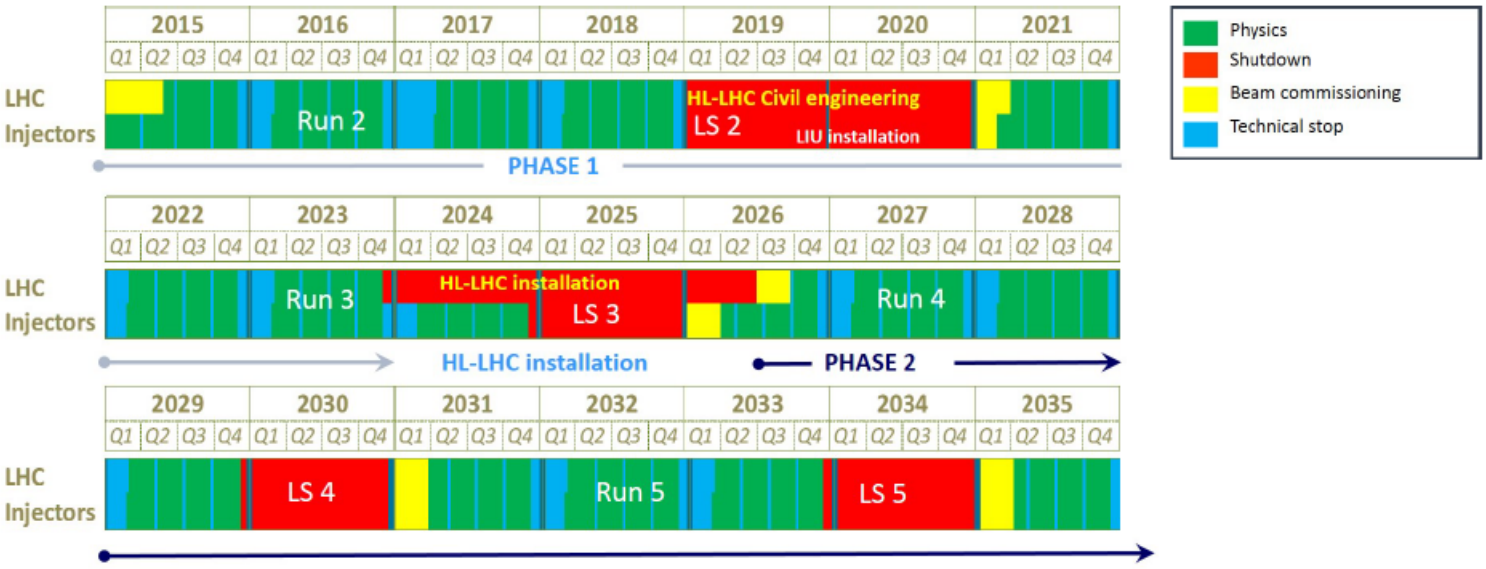


Figure 2.1 – LHC project planning from 2015 onward, showing the run phases and long shut-downs (LS) [1].

The High-Luminosity LHC (HL-LHC) project aims to increase the performances of the LHC by increasing the *luminosity factor* of the accelerator, which is a key indicator of its performance as this factor is proportional to the number of generated particle interactions over time. This increase in luminosity should allow the observation of new phenomena. LS3 is expected to induce peak luminosities of 5.10^{34} $cm^{-2}s^{-1}$ to $7.5.10^{34}$ $cm^{-2}s^{-1}$ in the ultimate performance scenario [1], [8]. The evolution of the luminosity factor across the years is shown in figure 2.2.

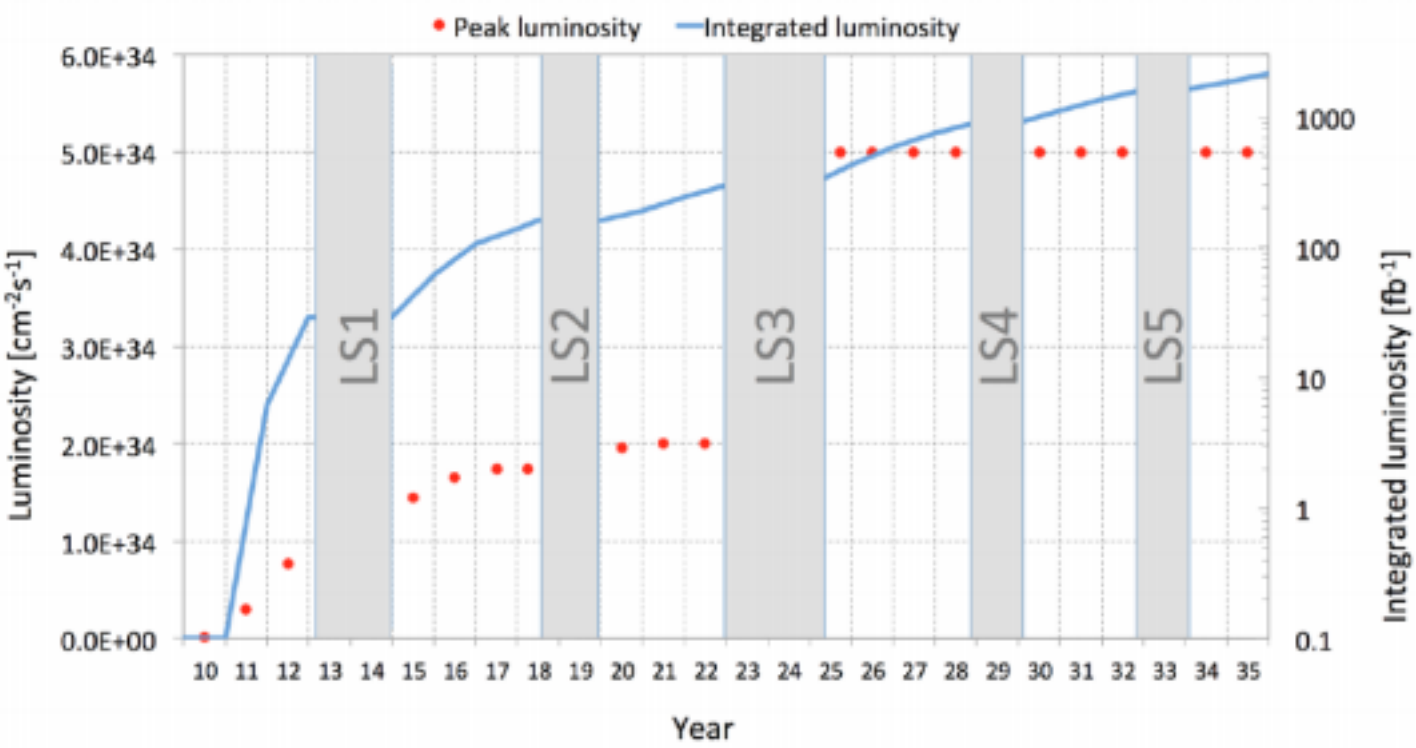


Figure 2.2 – Evolution of the peak luminosity and the integrated luminosity of the LHC across the years [2].

As part of the HL-LHC project, the CMS detector will be upgraded. This thesis falls under the *phase-2 upgrade* of the CMS detector towards the so-called *high-luminosity phase of the LHC* planned for 2026.

2.2 The Compact Muon Solenoid

The Compact Muon Solenoid (CMS) detector is a general purpose particle detector which is operated at the LHC at CERN. The CMS detector has been designed to study the Standard Model of particle physics and to search for new phenomena, beyond the Standard Model [3]. In 2012 CMS, with ATLAS, led to the discovery of the Brout-Englert-Higgs boson, the last missing piece of the Standard Model. As the name implies, the CMS detector utilizes a solenoid magnet in order to generate a magnetic field of 4T. The detector exhibits a length of 28.7m and a diameter of 15m and encompass a plethora of sub-detectors composed of particle tracking sensors and calorimeters. The CMS detector and its different layers are shown in figure 2.3.

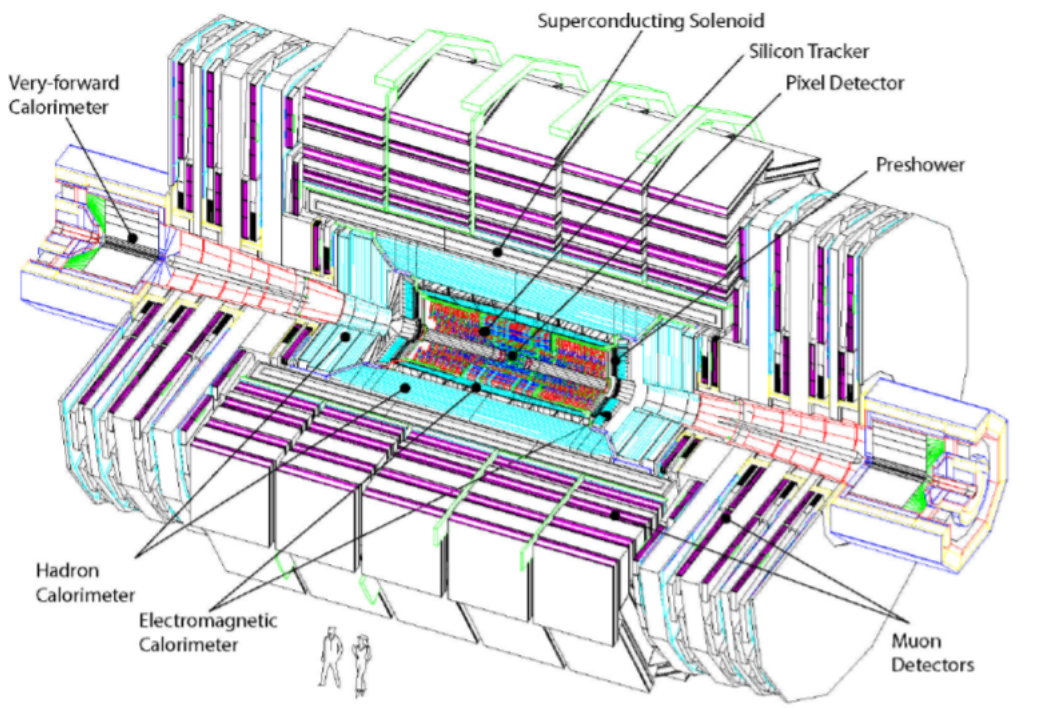


Figure 2.3 – The CMS detector and its different layers [3].

2.2.1 The Superconducting Magnet

The superconducting magnet used in the CMS detector is designed to provide a uniform magnetic field of 4T in a free bore of 6m of diameter and 12.5m of length, storing a maximal energy of 2.6GJ at full current [3]. The magnetic field generated by the solenoid is used to bend the trajectory of the charged particles generated by the collision. By reconstructing the trajectory of the particles using the *tracker sensors* (focus of this thesis), it is possible to determine the momentum p of the charged particles [9]. This is seen in figure 2.4.

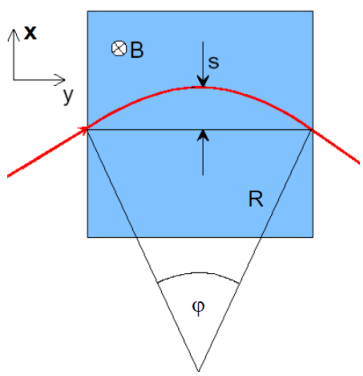


Figure 2.4 – Bending the trajectory of charged particles in the transverse plane to the magnetic field.

[9]

In the transverse plane to the magnetic field, p is given by equation 2.1 [9]:

$$p = qBR \tag{2.1}$$

Where q is the charge of the particle, B the intensity of the magnetic field and R the radius drawn by the particle. Equation 2.1 shows that *by tracking the trajectory of the particles, their momentum can be derived.*

2.2.2 The CMS trigger system

As the LHC runs at a frequency of 40MHz (collisions occur every 25ns), acquiring all the events is not viable in terms of computational resources and this high rate needs to be reduced by selecting only the relevant events. A two-level trigger system is used to judge whether if an event is relevant or not based on the properties of the sensed particles. The Level-1 trigger (LV1) is controlled at the front-end side, in the electronics of the particles detectors. If the collision has been considered as relevant, a Level-1 *Accept* signal is sent to acquire the complete data from the sensors, else the data is erased. This allows a reduction of the event rate from 40MHz down to several hundred kHz [10]. Then, as the event rate has been reduced, a High-Level Trigger (HLT) process can be applied, using more complex sub-sampling schemes to reduce the event rate even more, down to 100Hz.

2.2.3 The sub-detectors

The CMS detector is composed of four sub-detection stages: the tracker, the electromagnetic calorimeter, the hadron calorimeter and the muon tracker. A schematic cross-section of the CMS detector is shown in figure 2.5.

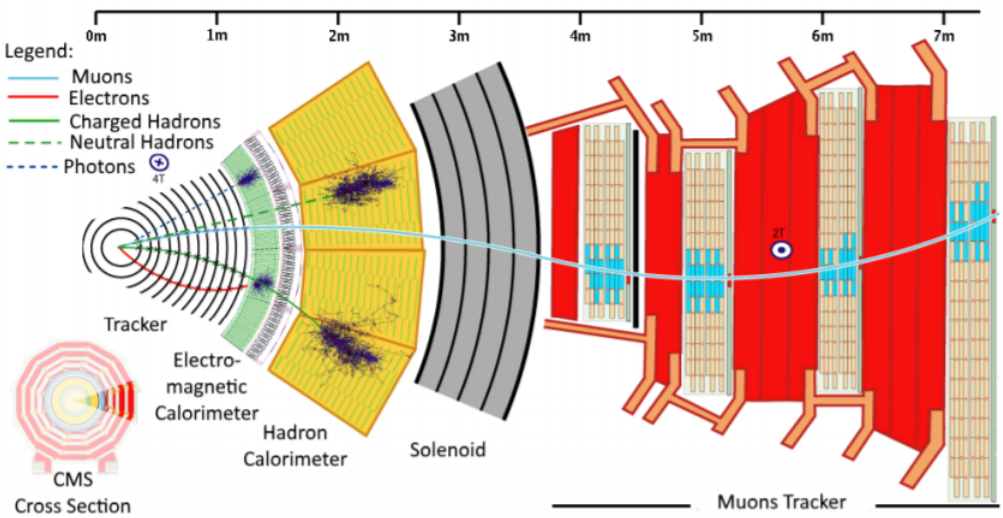


Figure 2.5 – Cross-section of the CMS detector showing the sub-detection stages. [11]

Starting from the collision point, the particles cross the Silicon Tracker, designed to provide a precise measurement of the charged particle trajectories. Then, the electromagnetic calorimeter measures the energy of electrons and photons while the hadron calorimeter measures the energy of hadrons (protons, neutrons,...). Finally, located outside the

solenoid, the last sub-detector is the Muon Tracker, which exclusively detects muons which are the sole particles able to pass through the previous layers [10]. The Silicon Tracker, which is the subject of this master thesis, is made of several layers of Silicon sensors [1]. Like the other sub-detectors, it is composed of a barrel part closed by two endcaps. An inside view of the current CMS Silicon Tracker is shown in figure 2.6.

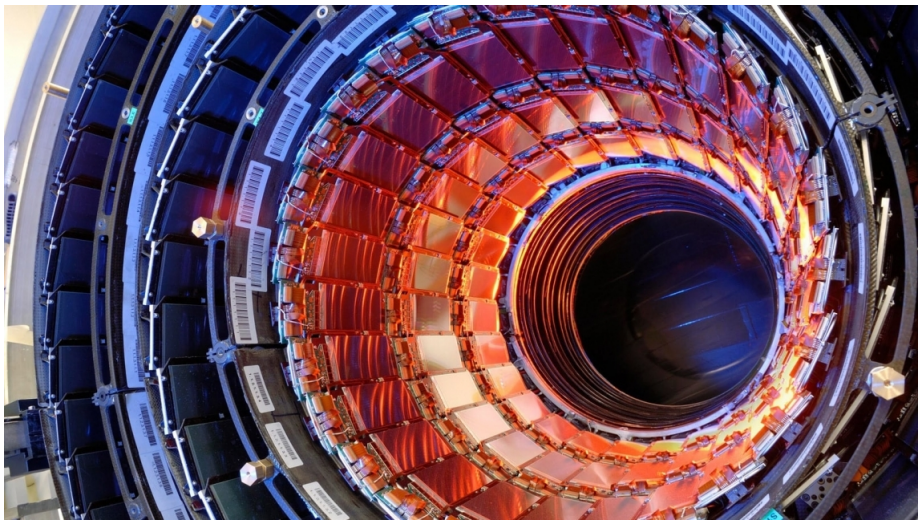


Figure 2.6 – Inside view of the current CMS Silicon tracker

2.2.4 The Phase-2 upgrade of the CMS Silicon tracker

As part of the HL-LHC project, the Silicon tracker of the CMS detector needs to be upgraded. The previous Silicon tracker was operating at instantaneous luminosities of 10^{34} cm^{-2}s^{-1}. However, *its performance is expected to degrade* due to radiation damage induced by the luminosity levels that the HL-LHC will exhibit. Before the start of HL-LHC, this Silicon tracker must be replaced due to the significant degradation that the current Silicon tracker would suffer in those extreme conditions. Among the different types of Silicon sensors used in CMS, the present project studies the so-called *2S Silicon strip sensors*, which will operate at $-35°$C in order to limit the effect of radioactivity on their performances [1].

2.2.5 The new 2S sensor modules

As said earlier, this thesis studies the Two-Strip (2S) sensor modules which are strip Silicon sensors. The 2S modules operate in the outermost layers of the Silicon tracking region of the CMS detector, called the outer tracking region. They are composed of two Silicon strip sensors separated by a spacer and are controlled by the so-called service hybrid (flexible PCB) [1]. A mechanical view of the 2S module in shown in figure 2.7.

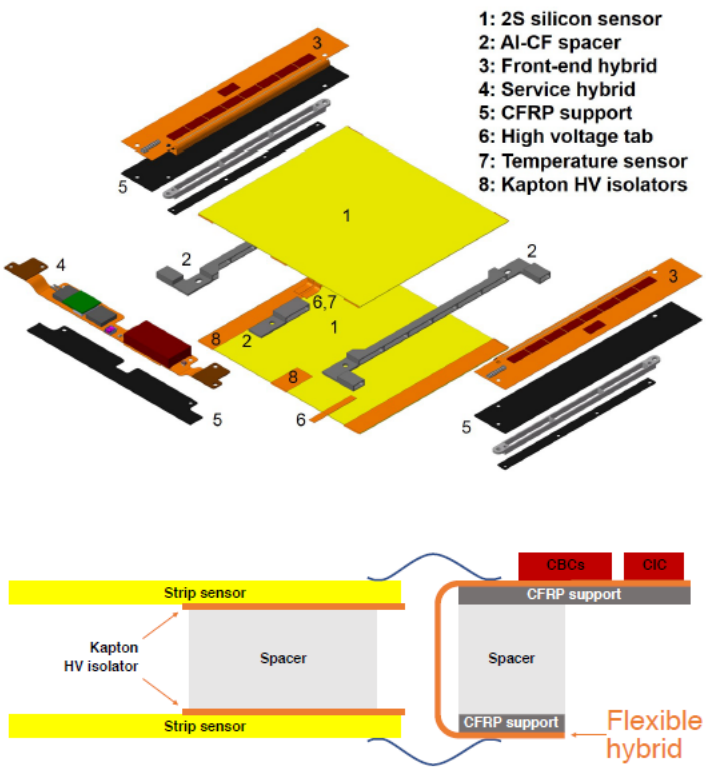


Figure 2.7 – Mechanical view of a CMS 2S module.
[1]

Each 2S Silicon sensor is composed of 2032 P-N junction strips with a total *active area* (depleted region at nominal reverse-bias voltage) of 90cm^2. The upper and lower sensors are read-out by eight ASICs (called the CBC3 chips) used to correlate the signals from the upper and the lower sensors to form trace segments called stubs. Their data is collected by the so-called Concentrator IC (CIC) chip and sent through optical fibre to the L1 trigger system and the computational facilities.

2.3 Contribution of this thesis to the new 2S modules

The IIHE is expected to build more than 2500 2S modules in their new class-7 clean room. As the 2S modules operate at a temperature of $-35°$C, their robustness to temperature cycles must be validated after the assembly of the modules. In particular, it is of interest to characterize the *current versus voltage* (I-V) and *capacitance versus voltage* (C-V) curves of the silicon sensors to verify if the full-depletion voltages are within specifications. In order to proceed to those characterizations, **a custom testing system for the new 2S modules must be designed to enable an automated testing of the 2S Silicon sensors**.

The design of such electronics system is a challenge as the measurement device should, in the ideal scenario, be operated at low temperatures ($-35°$C) inside industrial fridges (to minimize the amount of cabling through the fridge walls), the design must be finished

under *tight time constraints* and the produced equipment must remain *low-cost* while exhibiting the precision performances needed to characterize the sensors. This thesis aims to design, implement and experimentally validate such automated testing system that will be used at the IIHE to measure, under controlled temperature constraints, the I-V and C-V curves of the 2S sensors in order to approve their deployment for the phase-2 upgrade of the CMS detector at CERN.

2.4 Conclusion

This chapter described the overall context in which the thesis takes place. It has been seen that the CMS detector needs an upgrade to attain the performances expected from the HL-LHC project. As part of this upgrade, the new state-of-the-art 2S tracker modules will be assembled at the IIHE, asking for the development of an automated testing system enabling the characterization of the modules via I-V and C-V curve measurements. This master thesis project aims to build such system which will allow an automated characterization of the produced modules which is a key step towards their deployment at CERN.

Chapter 3
Working principle of Silicon strip sensors

In this chapter, the working principle of Silicon strip sensors and the layout of the CMS 2S modules will be described.

3.1 General overview

Figure 3.1 shows an example of a previous generation CMS Silicon strip sensor module (so-called *phase-0* sensor).

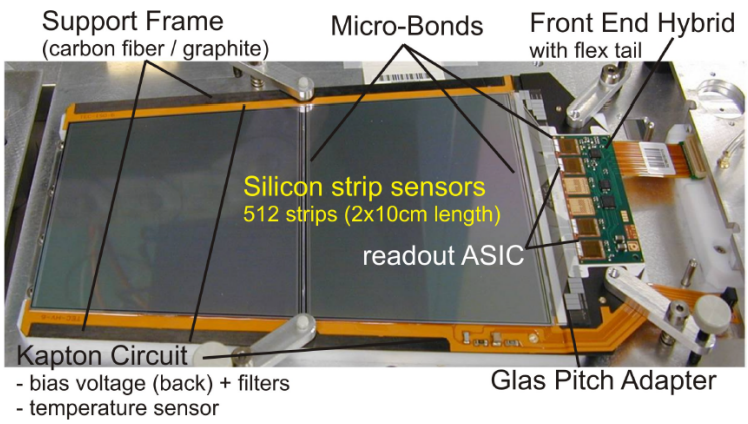


Figure 3.1 – An old *phase-0* Silicon strip sensor module. **Dimensions**: 30 × 10cm

The sensor modules are composed of the Silicon sensors themselves, a biasing circuit and the read-out ASICs which will read the charge accumulated on each strip due to charged particles passing by. Figure 3.2 shows the cross-section of a Silicon strip sensor.

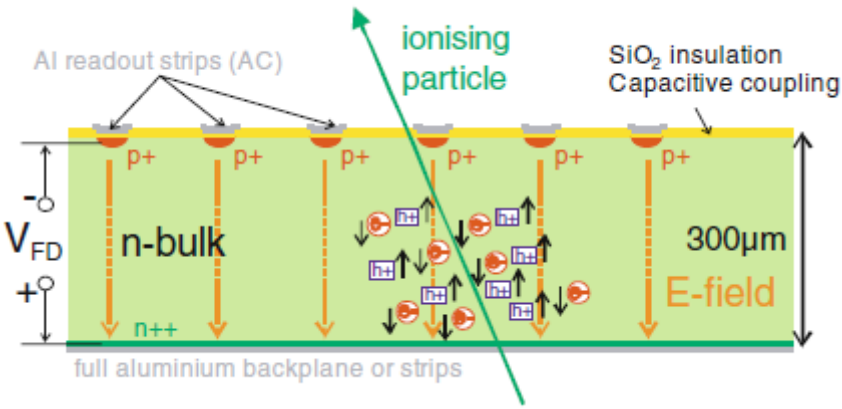


Figure 3.2 – Cross-section of a Silicon strip sensor [4].

The sensing principle is the following: the sensor is composed of P-N junctions, formed by $p+$ strips in a n bulk for the example of figure 3.2. Each P-N junction is reverse-biased by applying a voltage V_{FD} between the bias ring and the backplane. When a charged particle crosses the sensor, electron-hole pairs are produced. Those charges are then collected on the strip terminals and are AC-coupled to the read-out electronics.

In the next sections, the physical properties of the sensors will be detailed.

3.2 Silicon properties

3.2.1 Why using Silicon?

In particle physics, Silicon is not the sole material used for particle detection as gaseous detectors also exist. But using Silicon for particle tracking is highly desired as Silicon exhibit a higher material density than gaseous detectors, leading to orders of magnitude more electron-hole pair generated within the same volume ($\sim 3 \times 10^4$ e-h pairs in 300μm thick wafer) [5]. In addition, Silicon detectors have a higher energy resolution than gaseous detectors ($\sim$ 3.6 eV to produce an electron-hole pair v.s $\sim$ 30 eV in gaseous detectors) [4]. Furthermore, the particle signal detection in Silicon sensors is faster ($\sim$ 10 ns) due to the higher mobility of electrons and holes [4]. From a technological point of view, fabrication methods are standardised and allow the forming of strip and pixel shapes on the wafers. They also allow the deployment of the bias resistors and decoupling capacitors on the sensor wafer.

3.2.2 Intrinsic properties

Silicon wafers can be modelled as single crystal materials exhibiting a highly periodic arrangement in their entire volume, resulting in a *periodic* potential throughout the material. By solving Schrödinger's equation in conjunction with a periodic potential model (e.g Kronig-Penney), allowed and forbidden energy bands for the electrons and holes are derived [12]. The low-energy band with the outermost electrons is called the *valance* band and the next energy band with the free electrons is called the *Conduction* band. Those two bands are separated by a forbidden energy band called the *band gap* (1.12 eV for Silicon). In an intrinsic Silicon material, the electron and hole concentration (n_i and p_i) are equal. Furthermore, the product of electron and hole concentration is constant at thermal equilibrium, even if doping atoms are introduced (equation 3.1).

$$n_i p_i = n_0^2 \tag{3.1}$$

Also, the occupation probability for an electronic state is given by the Fermi-Dirac distribution (equation 3.2), following Pauli's exclusion principle [13]. Doping the semiconductor will shift the Fermi energy level and the probability of state occupancy accordingly.

$$f(E) = \frac{1}{1 + e^{\frac{E - E_f}{k_b T}}} \tag{3.2}$$

In order to have P-N junctions, doping must be introduced.

3.2.3 Introducing doping

Doping is introduced by adding donor or acceptor impurity atoms. Donor atoms from group V will make the *free electron* concentration larger than *hole* concentration and vice-versa for group III acceptor atoms. Adding donor atoms will shift the Fermi energy level towards the conduction band and form a **N-type** semiconductor material while adding acceptor atoms will shift the Fermi energy level towards the valence band and form a **P-type** semiconductor. Figure 3.3 shows the introduction of an Arsenic atom into the Silicon lattice. At sufficiently high thermal energies, a conduction electron is liberated.

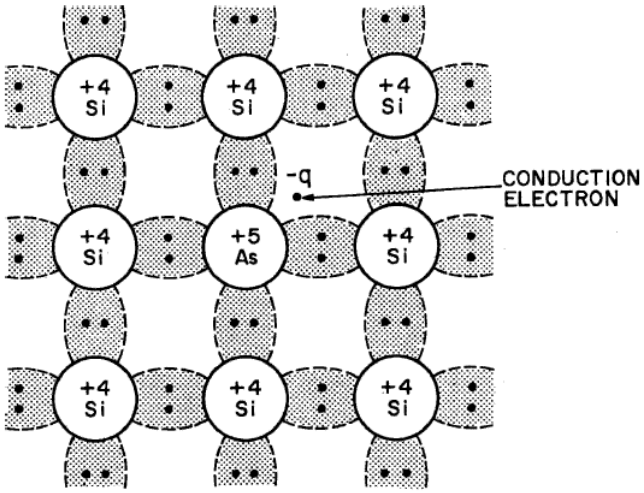


Figure 3.3 – Introducing Arsenic into the Silicon lattice.
[13]

3.3 The P-N junction

3.3.1 Abrupt change model

The Silicon strip sensors of the *phase-2* upgrade are composed of P-N junction strips formed by *n-type* implants in a p bulk. Without any biasing, electrons from the n side diffuse to the p side and holes from the p side diffuse to the n side such that the net positive and negative charges in the ionized region induce an *electric field* (and hence a *voltage barrier*) which counteracts the diffusion process. Figure 3.4 shows the P-N junction abrupt change model.

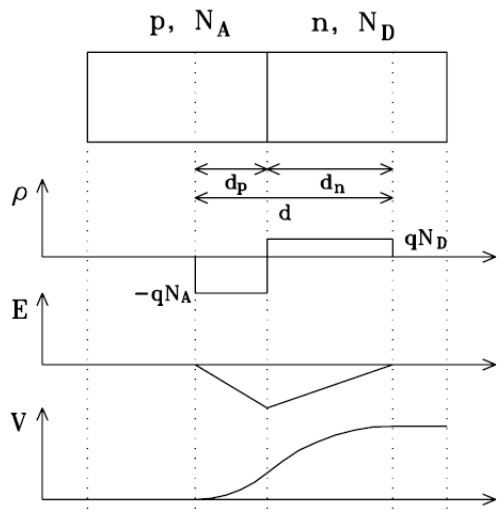


Figure 3.4 – P-N junction following the abrupt change model. From top to bottom: geometric model of the junction, charge density ρ, electric field E and electric potential V.

[13]

Positive and negative charge densities (ρ) are induced in the depletion region (where N_a and N_d are the acceptor and donor concentrations). By integrating Gauss's law ($\nabla\vec{E} = \frac{\rho}{\epsilon}$), the electric field inside the space-charge zone is found [5]. The *potential barrier* is then derived by integrating the electric field along the depletion region.

Using this model, equation 3.3 gives the potential barrier at thermal equilibrium without the application of a bias voltage (where n_i is the intrinsic carrier concentration).

$$V_{bi} = \frac{k_b T}{e} \ln \frac{N_a N_d}{n_i^2} \tag{3.3}$$

When a *reverse-bias voltage* V_R is applied, the width W of the depletion region increases following equation 3.4.

$$W = \sqrt{\frac{2\epsilon(V_{bi} + V_R)}{e} \frac{N_a + N_d}{N_a N_d}} \tag{3.4}$$

3.3.2 Determining the reverse-bias voltage needed to attain full-depletion

The sensors must be operated at full depletion as the space charge zone is at maximal width W in this condition, leading to a maximal particle sensing volume. The P-N junction can be seen as a parallel plate capacitance as the space-charge zone acts as an insulator between the terminals of the device. Using the junction width W, a capacitance C_j is associated to the P-N junction following equations 3.4 and 3.5.

$$C_j \propto \frac{1}{W} \propto \frac{1}{\sqrt{V_{bi}}} \tag{3.5}$$

Furthermore, the electron-hole pairs thermally created in the depletion region volume ($\propto W$) induce a reverse-bias *leakage current* I_{leak} following equation 3.6.

$$I_{leak} \propto W \propto \sqrt{V_{bi}} \tag{3.6}$$

When increasing the reverse-bias voltage, the width W stops increasing at a certain point corresponding to *full-depletion*. At this point, a plateau appears in the C-V and I-V curves. Thus, by measuring the evolution of C_j and I_{leak} in function of the reverse-bias voltage, it is possible to determine the reverse-bias voltage needed to reach full-depletion. Figure 3.5 shows the C-V curves of typical Silicon sensors. Full-depletion is achieved when the plateaus are reached.

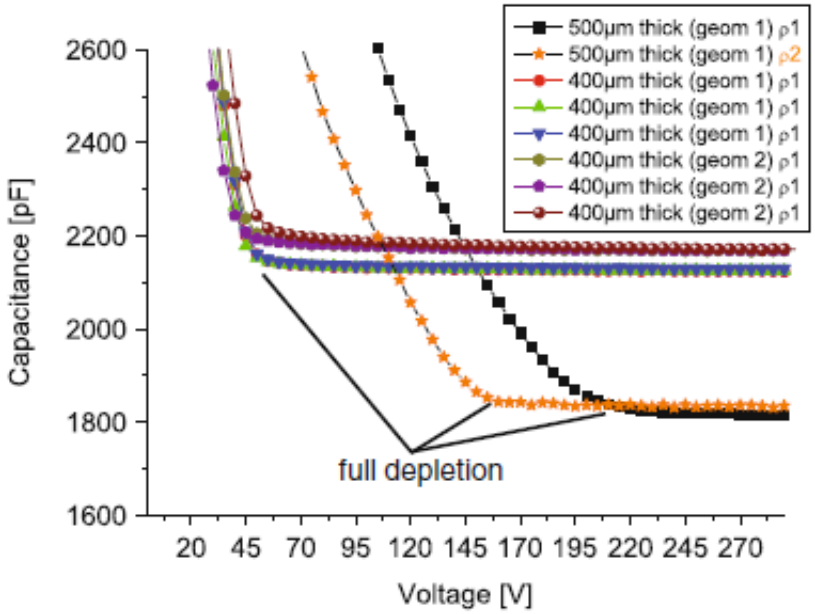


Figure 3.5 – C-V curves of typical Silicon sensors
[4]

3.3.3 Deviation from the ideal P-N junction model

Real-world sensors deviate from those ideal properties due to several factors. At higher reverse-bias voltages, *junction breakdown* takes place due to the *Zener* and the *avalanche* effects. The *Zener* effect can be understood as the tunneling between the valance and the conduction band due to the high electric field and the avalanche effect is due to electrons and holes moving across the depletion region with enough energy to create other electron-hole pairs by colliding with atomic electrons [12].

Furthermore, the sensor bulk is contacted using a metallic backplane which could form an undesired *Shottky* diode. To counter this effect, the contacting zone of the bulk is highly doped to allow good Ohmic contact between the metallic backplane and the bulk.

Other unwanted effects can be noted such as the parasitic capacitances between the strips or the non-uniformity of the electric field inside the sensor at lower reverse-bias voltages (see figure 3.6 and **appendix E**) [4].

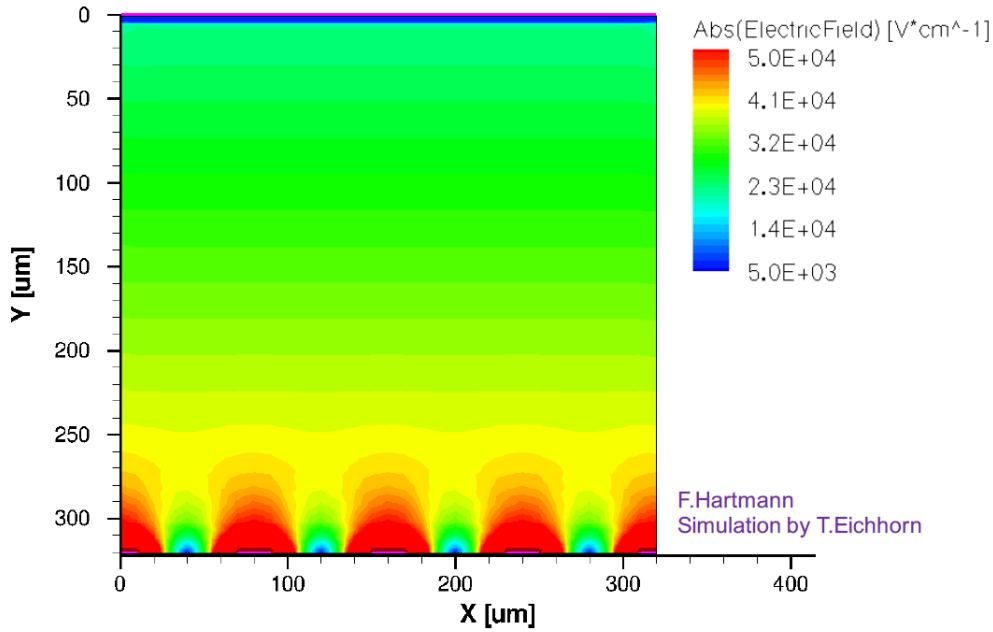


Figure 3.6 – **Typical electric field inside a Silicon strip sensor**. The maximal electric field is reached at the strip implant locations (red regions). [4]

3.4 Forming a tracking detector

Figure 3.7 shows the typical arrangement of a track detector. P-N junctions are formed by implanting parallel strips into the bulk. Each strip is connected through a *polysilicon* bias resistor to a *bias ring* in order to isolate the induced charge generated on each strip by particles passing by. The bulk is connected to an aluminium backplane. The reverse-bias voltage is then applied between the backplane and the bias ring.

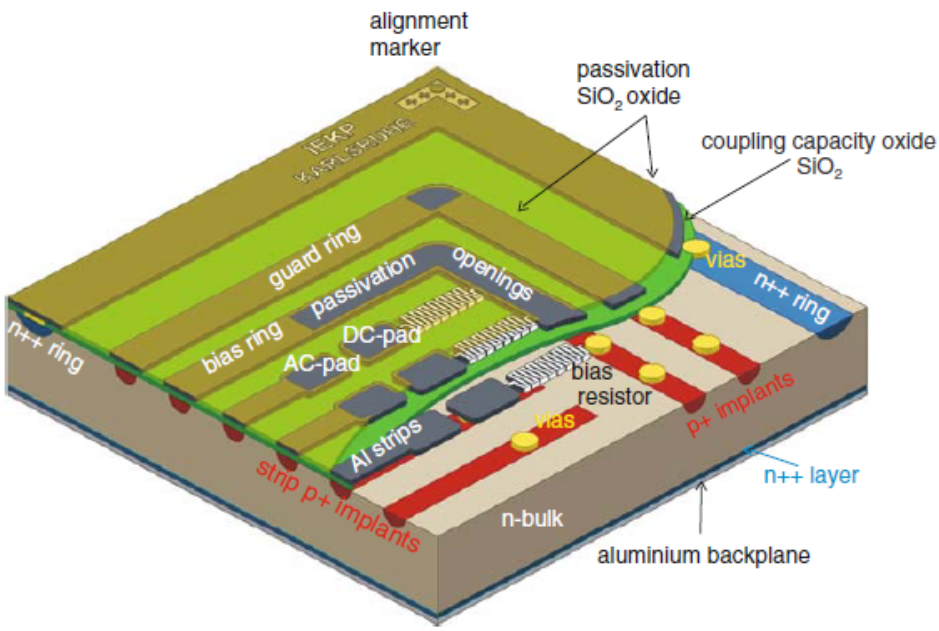


Figure 3.7 – Typical arrangement of a track detector [4].

The induced charge on the surface of each strip is then converted to a voltage signal by a charge-to-voltage amplifier. The leakage current is also filtered using coupling capacitors as seen on figure 3.8.

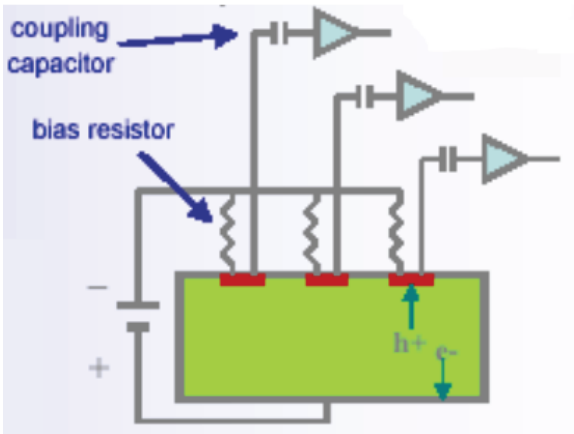


Figure 3.8 – Charge to voltage conversion circuit.
[5]

For the CMS tracker upgrade, the voltage signal from each strip is then read by *readout ASICs* (eight CBC3 chips and one concentrator CIC chip for each 2S module). By combining an upper and a lower sensor, *stubs*, which are linear approximation of the curved particle trajectory can be formed (see figure 3.9). Depending on the slope of each stub, *trigger signals* can be generated. Finally, the information from all the sensors is relayed to higher-level units which process the data.

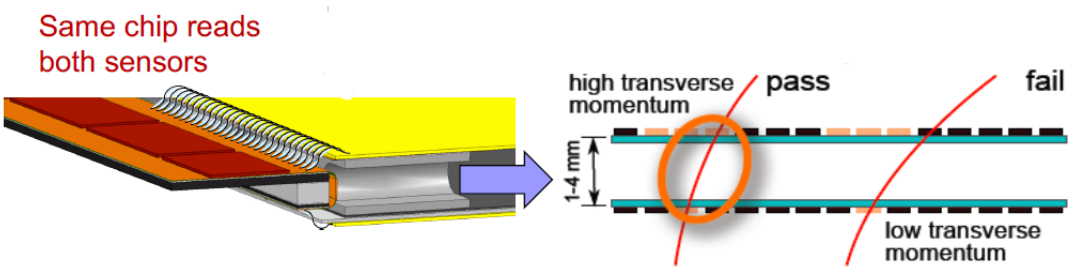


Figure 3.9 – Stub-forming principle used by the CMS 2S modules [5].

3.5 Conclusion

In this chapter, an overview of the working principle of Silicon strip sensors and the structure of tracking detectors has been detailed. The link between the junction width (determining the active volume of the sensor) and the junction capacitance and leakage current has also been given. This theoretical background will be used to model the sensor under test and to determine the full-depletion voltage of the sensors.

Chapter 4
High-level view of the system

In this chapter, a bird's eye view of the complete sensor characterization set-up will be detailed and the motivation behind each sub-system will be explained.

4.1 System architecture

The needed macro-blocks are the following:

- An industrial fridge (figure 4.1) to provide a light-tight environment and to perform experiments at different working temperatures, down-to −35°C.
- An integrated electronics system called the *Slow Control Board* (SCB, figure 4.2) allowing:
  - The monitoring of environmental data (temperature and humidity).
  - The generation of the high reverse bias voltage to deplete the Silicon sensors.
  - The measurement of the reverse-bias leakage current.
  - The measurement of the junction capacitances (using an external sine-wave generator).
  - The powering of the ASICs mounted on the sensor modules.
  - The real-time communication of the measurements to an external computer.
- An interface software that will be deployed on the external computer.

Figure 4.1 – The industrial fridge.

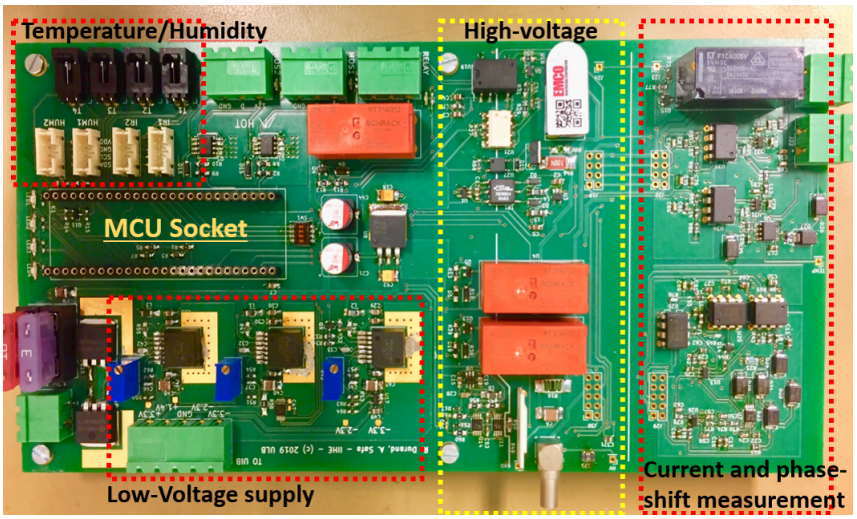


Figure 4.2 – Final design of the Slow Control Board used to characterize the Silicon sensors

Regarding the control software, an interface program must be written in C++ in order to be compatible with the so-called *phase2ACF* software suite from CERN [14]. The interconnection between the different macro-blocks is shown in figure 4.3.

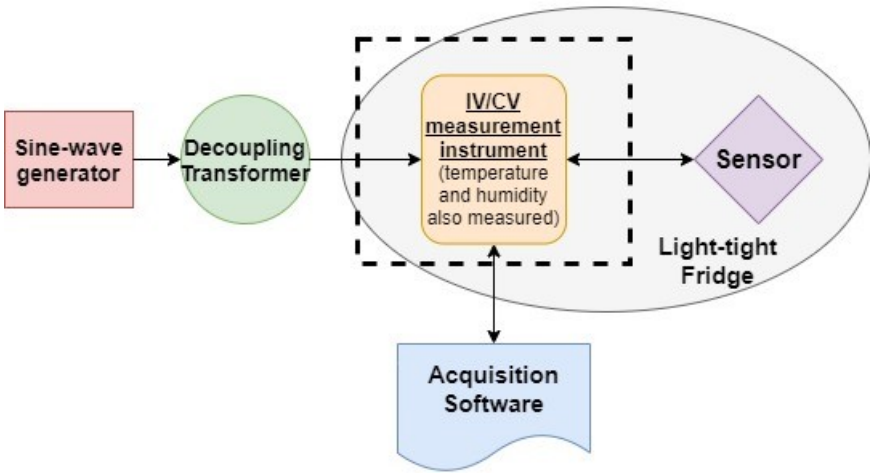


Figure 4.3 – **Interconnection between the macro-blocks composing the complete system.** The SCB and the tracker sensor to be characterized are placed inside the fridge, an external sine wave is provided by an isolated signal generator, the SCB communicates with the external software suite in real-time.

4.2 Slow Control Board Topology

4.2.1 Temperature and humidity sensors

The design of the SCB is expected to provide a complete monitoring of the environment inside the fridge during the characterization of the sensor modules. As the Silicon sensors are placed inside the fridge during the tests, condensation must be avoided during

the characterization process of the sensors because of the damage that it could induce on them. Condensation can be prevented by monitoring the humidity and the temperature of the air inside the fridge. The design of the SCB incorporates a pair of temperature and humidity sensors in order to predict any potential condensation.

Condensation can appear if the temperature inside the fridge drops below the dew point temperature. Assuming a constant air pressure inside the fridge, the dew point temperature T_{dp} can be found using the Magnus equation [15]:

$$T_{dp} = \frac{\lambda(\ln[\phi] + \frac{\beta T}{\lambda + T})}{\beta - (\ln[\phi] + \frac{\beta T}{\lambda + T})} \tag{4.1}$$

where ϕ is the relative humidity at the temperature T. The Magnus parameters for a temperature range of $-45°$C to $60°$C are given in table 4.1.

β	λ
17.62	243.12°C

Table 4.1 – **The Magnus parameters.** For a temperature range of $-45°$C to $60°$C.

4.2.2 High-voltage generator circuit

The SCB needs to incorporate a low-ripple high-voltage generation circuit in order to reverse bias the Silicon sensors upto and beyond full depletion. The Silicon sensors need to be characterized by their I-V and C-V curves. This high-voltage generator circuit will thus be expected to be settable, demanding the deployment of a regulator in the micro-controller firmware for the high-voltage generation circuit.

4.2.3 Current and capacitance measurement circuits

A current measurement circuit must be implemented to monitor the current consumed by the sensors in function of the reverse bias voltage which is applied. This will allow the generation of the I-V curves. Furthermore, the current measurement circuit will also be used to proceed to the capacitance measurements. The capacitance measurement circuit will be comprised of a external sine wave generator and a phase-shift measurement circuit which will provide a full capacitance measurement solution when combined with the current measurement circuit stated above.

4.2.4 Power management blocks

In order to power the ASICs mounted on the sensor modules, a power management circuit that will generate the power rails (-3.3V, -2.3V, 1.4V and 3.3V) needed for the ASICs must be deployed on the board. In addition to that, a voltage and current measurement circuit needs to be implemented to monitor the power consumed by the ASICs.

4.2.5 Block diagram of the slow control board

A block diagram of the slow control board is shown in figure 4.4. The circuit blocks are controlled by a micro-controller (CY8C5888LTI, **see appendix F for more details**).

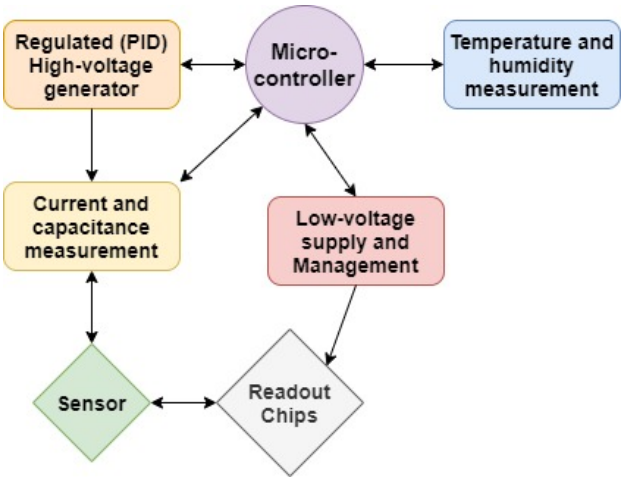


Figure 4.4 – **Block diagram of the SCB.** The central micro-controller manages the hardware blocks. The diagram also shows the interconnection between the high voltage generator and the current and capacitance measurement circuit.

4.3 Interface software

An interface software has been written during the project (figure 4.5) and is used to control the SCB and to write the measurements to user-defined *.csv* files. The software core is written in *C++* and the Graphical User Interface (GUI) is written in *Python*. The GUI provides text fields where the user can specify the name of the files to which the measurements are saved. It also provides temperature, humidity and dew point temperature monitoring. Finally, it provides a view of the acquired C-V or I-V curves to enable a fast visual analysis by the user.

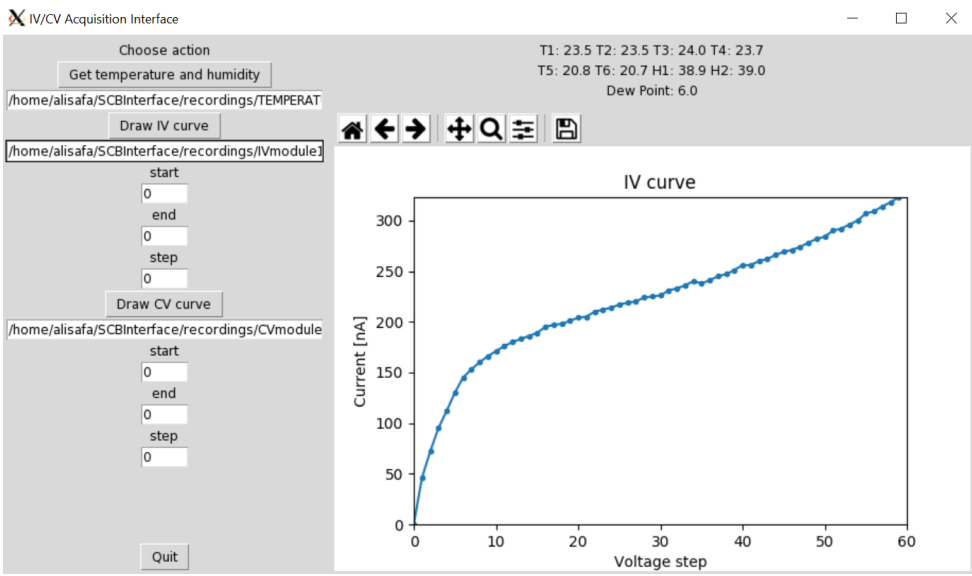


Figure 4.5 – **View of the acquisition software**. An IV curve has been measured and plotted for the sake of illustration. The six temperature readings (in degree Celsius), the two relative humidity readings (in %) and the dew point temperature reading (in degree Celsius) are also shown.

4.4 Conclusion

In this chapter, a high-level overview of the test system that needs to be designed has been given. The functionalities expected to be implemented by the SCB have also been shown. The interface software has also been presented.

At the start of this thesis, a first version of the SCB was already available [16] although **untested**, with **no firmware** and **without a capacitance measurement circuit** (for C-V curves). After board assembly and debugging, it was found that the current measurement circuit (for I-V curves) already available was **not appropriated** and further **modifications** needed to be made all over the board.

Regarding the SCB hardware design, the author of this master thesis mainly contributed to:

- The high-voltage generator regulation.
- The current measurement circuit (for I-V curves).
- The capacitance measurement circuit (for C-V curves).
- The debugging and repair of existing design mistakes in the first version of the SCB.
- The re-design of a second version of the board (figure 4.2).

In addition, the author conducted:

- Complete firmware design.
- Complete interface software design.
- Experimental validation of the system using real-world tracking sensors.
- Presentation of the project during internal CMS meetings.
- Presentation of the project to the community at an **international level** (TREDI 2020 "Trento" Workshop, Vienna, Austria. See appendix H).

In the next chapter, the design of the high-voltage generator circuit deployed on the SCB will be presented.

Chapter 5
Design of the low-ripple high-voltage generator

The Silicon sensors to characterize are expected to reach their full depletion state at reverse-bias voltages of several hundred Volts. As the sensor characterization is done through the generation of I-V and C-V curves, the reverse-bias voltage needs to be arbitrary settable by the central micro-controller unit. Furthermore, a low output ripple is desired in order to generate reliable characterization curves.

This chapter presents the design of a digitally regulated, low-ripple, high-voltage generator that will be used to reverse-bias the Silicon sensors.

5.1 Circuit design

The high-voltage generator circuit is composed of three blocks (in addition to the micro-controller): an isolated *pulse-width modulation* (PWM) to high-voltage conversion circuit, an output low-pass filter and an attenuator/anti-aliasing filter circuit allowing the acquisition of the high-voltage by the ADC peripheral of the micro-controller. Figure 5.1 shows a block diagram of the high-voltage generator circuit.

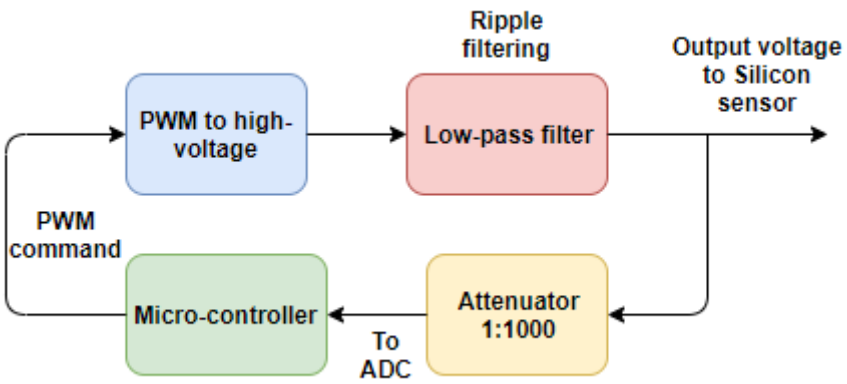


Figure 5.1 – High-voltage generator block diagram.

In the following sections, the implementation of each block will be described.

5.1.1 PWM to high-voltage converter circuit

Figure 5.2 shows the schematic of the isolated PWM to high-voltage converter circuit. The HV_PWM (PWM command) signal is generated by the micro-controller. By modulating the width of this signal, the base voltage provided to the transistor $Q6$ can be changed

(through to the low-pass filter formed by *R29*, *R31*, *C17* and *C54*) which results in a change in the *HV_CTRL* voltage value. This latter signal is provided to the *CNTRL* pin of the *A10P-12* high-voltage generator module which allows the setting of the positive and negative high-voltage outputs (*HV+* and *HV-*). Isolation is provided by the opto-coupler *TLP351* (*U21*) and the DC to DC converter *ISH1212A* (*U19*). The *A10P-12* high-voltage generator module is internally composed of an oscillator coupled to a transformer and rectifier and can provide up to 1mA of current which is enough as the maximum leakage current of the sensors is expected to be in the order of micro-amps.

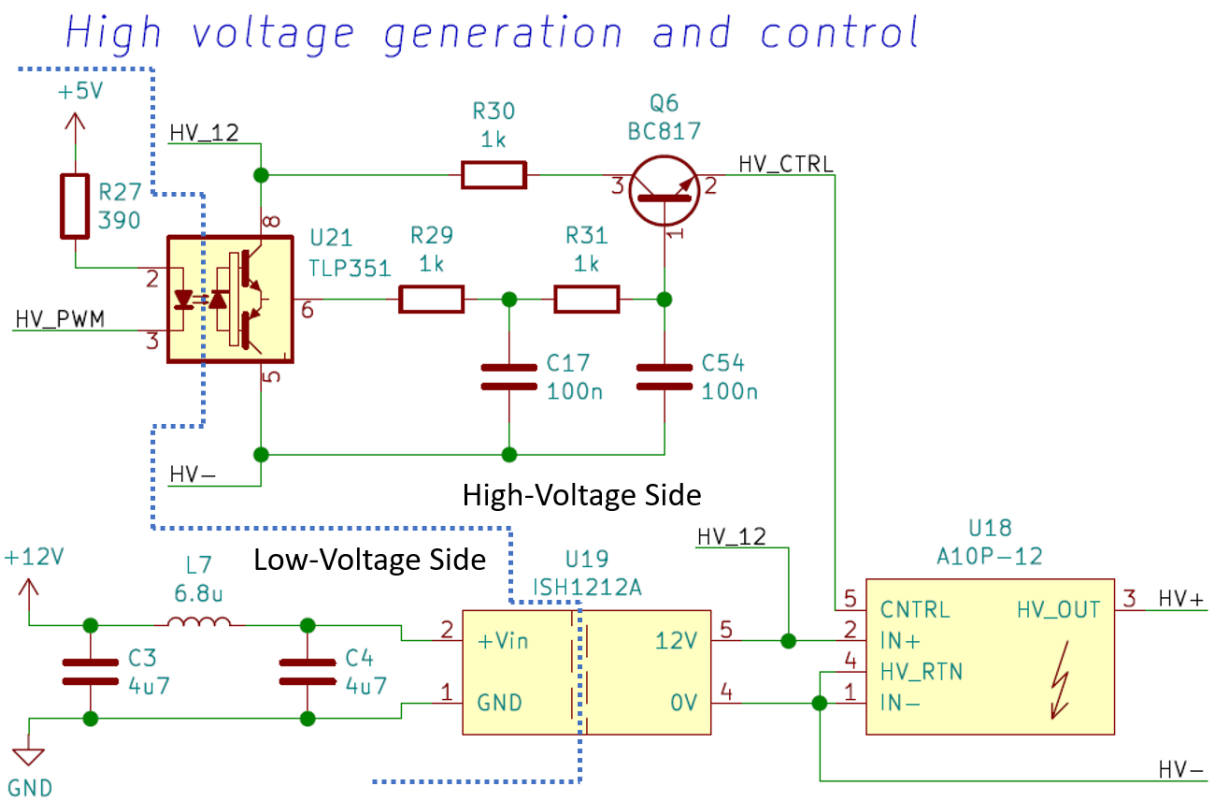


Figure 5.2 – **The isolated *PWM* to high-voltage generator circuit.** Isolation against the high-voltage side is provided by the *TLP351* (*U21*) opto-coupler and the *ISH1212A* (*U19*) DC to DC converter.

The low-pass filter formed by *R29*, *R31*, *C17* and *C54* is used to convert the *PWM* signal into a DC voltage depending on its duty cycle. Therefore, the *PWM* frequency must fall way after the cut-off frequency of the low-pass filter in order to minimize any induced ripple on the *CNTRL* line which would directly result in a ripple on the high-voltage output. Figure 5.3 shows the magnitude Bode plot of the low-pass filter.

By choosing a frequency of 25kHz for the *PWM* signal, the attenuation is −48dB which is enough in the present application.

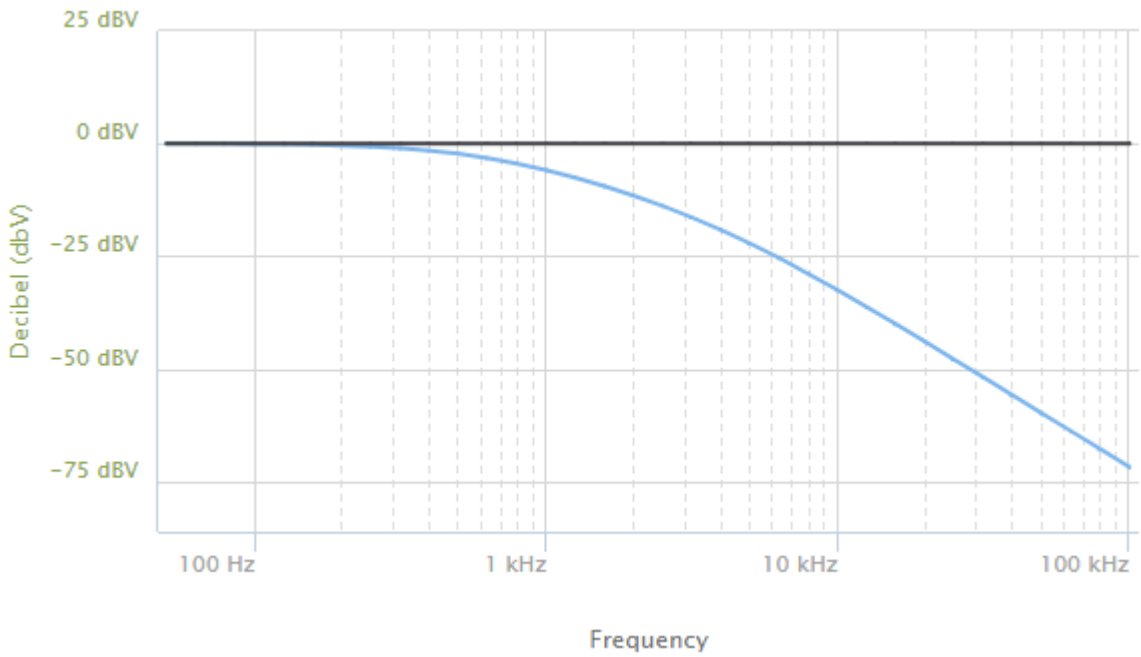


Figure 5.3 – **Magnitude Bode plot of the low-pass filter** The cut-off frequency is found to be around 600Hz.

5.1.2 Output ripple low-pass filter

In order to provide additional attenuation to any ripple that could occur, the filter shown in figure 5.4 has been used at the output of the high-voltage converter circuit.

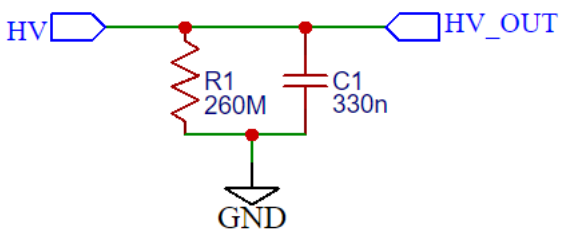


Figure 5.4 – Ripple filter.

The 260MΩ resistor is used to provide slow discharge of the filter capacitor while the 330nF capacitor is used to provide a low-impedance path to ground for any higher-frequency ripple.

5.1.3 Attenuator/Anti-aliasing circuit

In order to sense the high-voltage output by the ADC peripheral present in the micro-controller, the output voltage must be attenuated. Figure 5.5 shows the attenuator/anti-aliasing circuit.

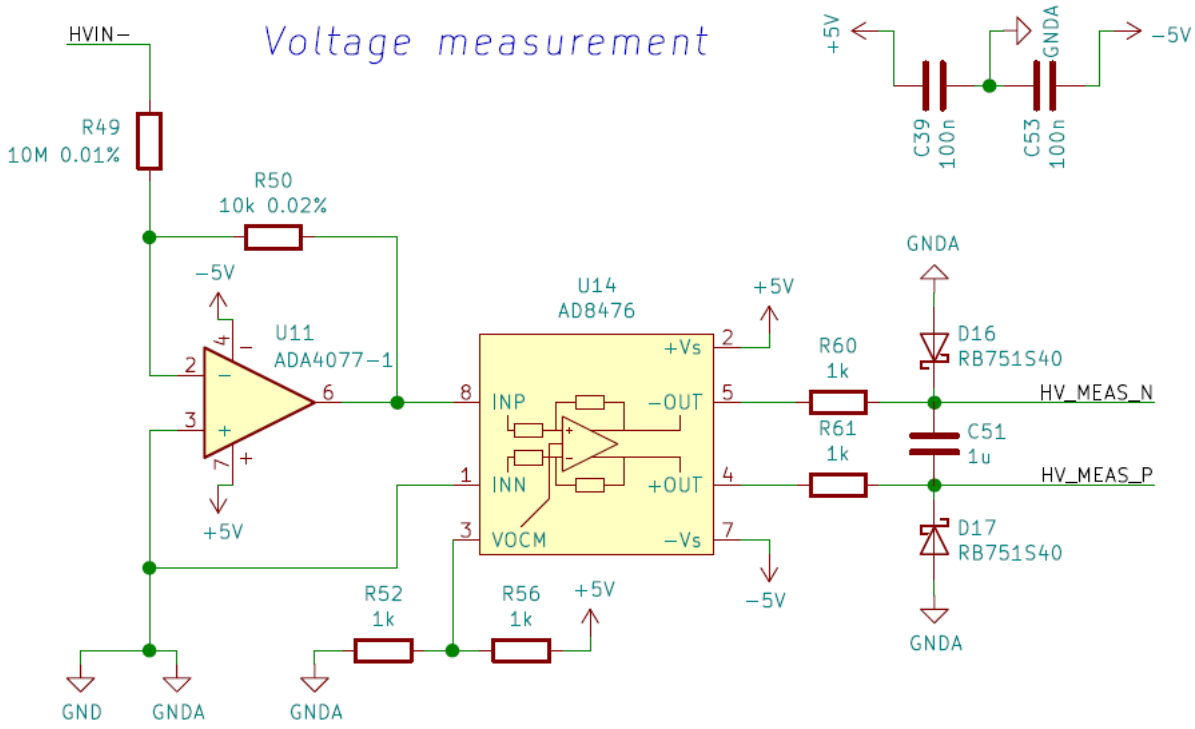


Figure 5.5 – Attenuator circuit.

The first stage of the circuit (*R49*, *R50* and *U11*) is composed of an inverting amplifier providing a gain of $\frac{1}{1000}$. The inverted and attenuated signal is then fed to a differential amplifier (*U14*) that acts as a buffer to drive a 16-bit $\Delta\Sigma$ ADC integrated in the micro-controller (**see appendix G**). The differential amplifier also provides another inversion to the signal which compensates the first stage, and an offset of 2.5V (using *R52* and *R56*) in order to meet the single-rail ADC coverage range. Input protection is also provided using two Schottky clamping diodes (*D16* and *D17*). Finally, a RC low-pass filter is also present (*R60*, *R61* and *C51*) with a time constant τ_{filter} given by equation 5.1.

$$\tau_{filter} = 2k\Omega \times 1\mu F = 0.002s \tag{5.1}$$

5.1.4 Digital regulation using the micro-controller

The micro-controller provides the analogue to digital conversion, the regulator and the *PWM* control signal. Using the ADC peripheral, the differential pair (*HV_MEAS_N* and *HV_MEAS_P*) on figure 5.5) carrying the attenuated high-voltage signal is fed to a 16-bit Delta-Sigma ADC. This latter has been chosen for its high-precision [17] as a fast sample rate is not required in the acquisition of a predominantly DC signal (other types of ADCs provide larger sample rates at the expense of precision).

Before designing the regulator, a model for the *PWM to voltage system* must be acquired. It has been experimentally found that providing *PWM* step-like commands to the converter circuit always resulted in first-order type responses $Y(t)$ which can be modelled using equation 5.2 (where A is the amplitude term, τ is the characteristic time constant

corresponding to the moment when the output reaches 63% of its final value and t is the time).

$$Y(t) = A(1 - e^{-\frac{t}{\tau}}) \tag{5.2}$$

By providing step commands starting at different equilibrium points, it has been also found that the *PWM to voltage* system became faster as the equilibrium point was set at a higher voltage (τ became smaller). This results in the fact that the pole of the system is pushed further to the negative side (left half-plane) in the complex plane as the equilibrium point is set to a higher voltage, making the system more and more stable in closed loop. A step response shown in figure 5.6 has thus been conducted by starting at an equilibrium point of 0V to take the worst-case scenario.

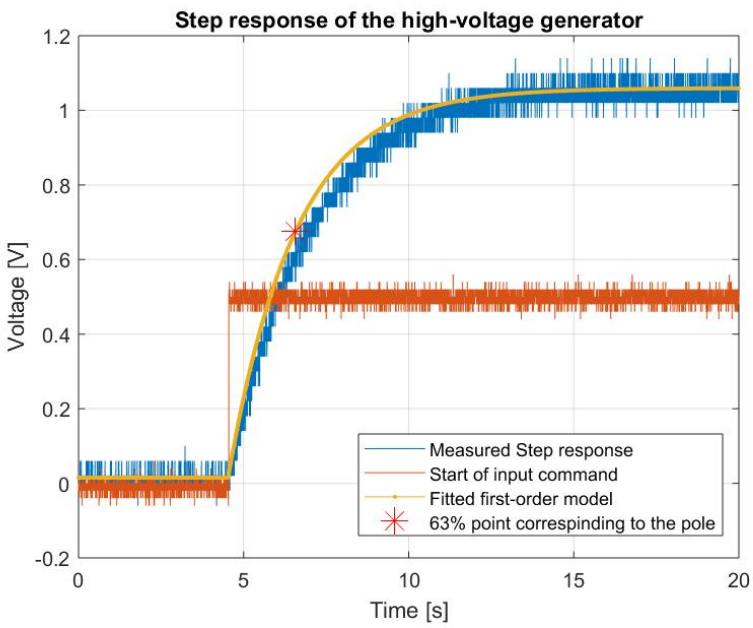


Figure 5.6 – **Step response of the *PWM to voltage* system.** Waveforms were acquired using an **oscilloscope** and exported in *.csv* into MATLAB. τ has been identified as 2.042 seconds.

A τ value of 2.042 seconds has been identified for the first order model. For the regulation, a classical *proportional–integral–derivative* (*PID*) filter has been selected because of its properties: the presence of an integrator allows the system to exactly reach the command value and the presence of a derivative channel provides a fast response to changes in the output error. Furthermore, as the *PID* controller is quite generic, it will be possible to fine-tune the controller to counteract behaviours omitted by the first-order model. The transfer function (Laplace domain) of a PID controller is given by equation 5.3.

$$G(s) = \frac{K_d s^2 + K_p s + K_i}{s} \tag{5.3}$$

The final coefficients of table 5.1 were experimentally found by tuning each parameters while looking at the output ripple histogram via an oscilloscope.

K_p	K_i	K_d
0.002 [1/V]	0.1074 [1/s.V]	0.002 [s/V]

Table 5.1 – ***PID* coefficient values.**

A theoretical approach such as *pole-zero cancellation* gives a similar set of coefficients. Indeed, $G(s)$ (equation 5.3) has two zeros and one pole. When put in series with the first order model, equation 5.4 is found.

$$Y(s)G(s) = \frac{A}{\tau s + 1}\frac{K_d s^2 + K_p s + K_i}{s} \tag{5.4}$$

The two zeros of $G(s)$ are given by equation 5.5.

$$z_{1,2} = \frac{-K_p \pm \sqrt{K_p^2 - 4K_d K_i}}{2K_d} \tag{5.5}$$

To cancel the pole of $Y(s)$, equation 5.6 must be satisfied.

$$\begin{cases} \frac{K_p}{2K_d} = \frac{1}{\tau} \\ K_i = \frac{K_p^2}{4K_d} \end{cases} \tag{5.6}$$

By fixing K_d to 0.002 sV^{-1}, K_p and K_i are respectively found as 0.002 V^{-1} and 0.00048 $s^{-1}V^{-1}$. Those coefficients are thus the same as found experimentally apart from K_i. In practice, a higher K_i value of 0.1074 $s^{-1}V^{-1}$ has been used as it gave rise to a lower ripple across the high-voltage range, in the expense of response speed. Figure 5.7 shows the *gain and phase margins* of the system with the coefficients of table 5.1. The gain margin is theoretically infinite and the phase margin is higher than 60° (good rule of practice).

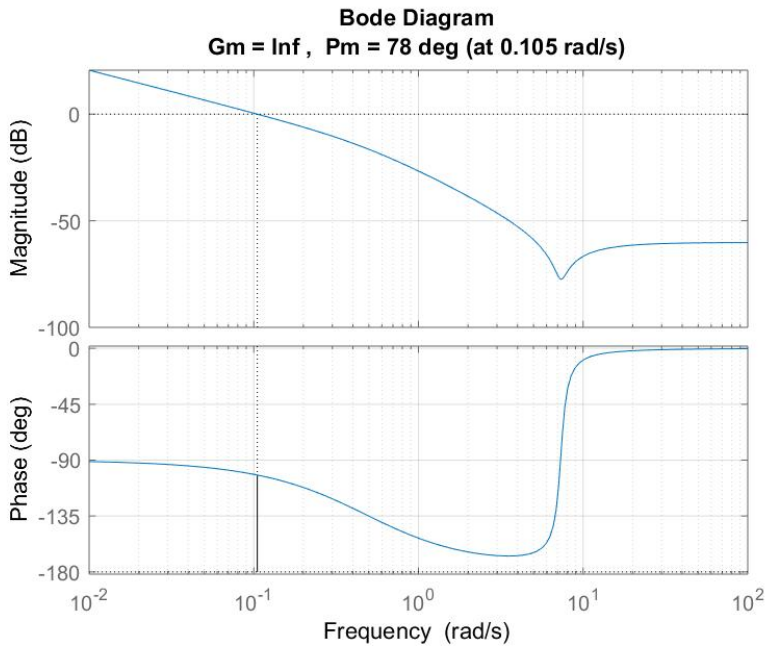


Figure 5.7 – **Gain and Phase margin of the regulated system.** Gm = ∞, Pm = 78°.

Furthermore, figure 5.8 shows the Bode diagram of the system in closed loop. As expected, the system behaves as a low-pass filter with strong attenuation (−60dB) near DC.

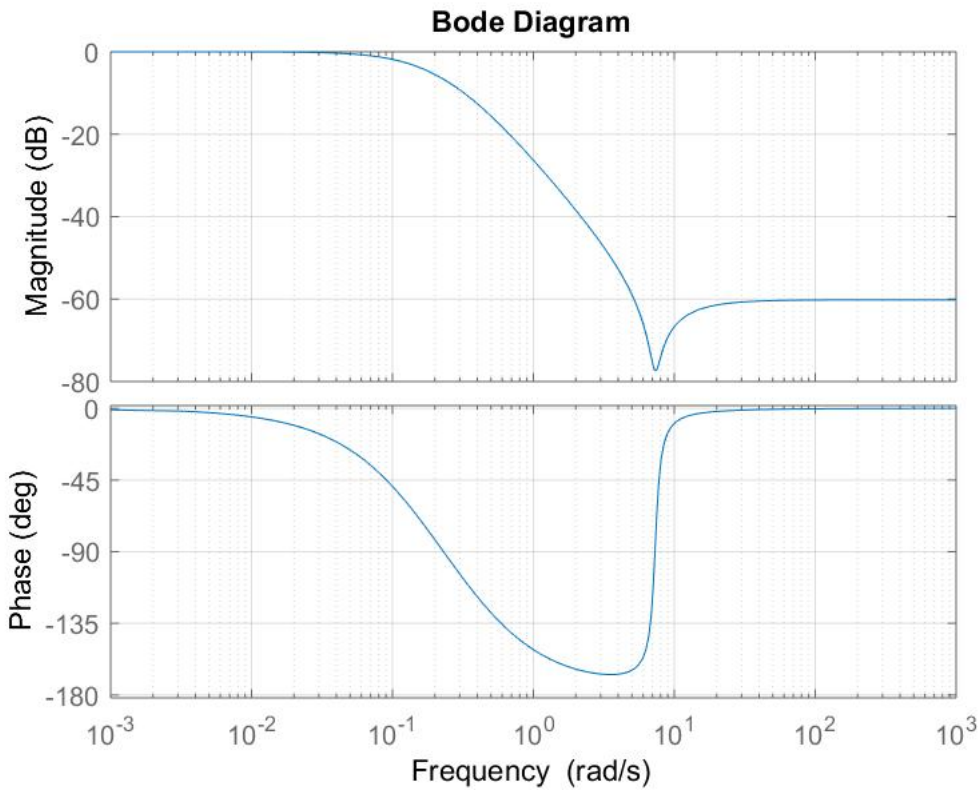


Figure 5.8 – Bode diagrams of the system in closed-loop.

This digital regulator has thus been implemented in the micro-controller firmware. In the next section, the ripple performances of the high-voltage generator are discussed.

5.2 Ripple performance

The ripple performance of the regulator used within the high-voltage circuit can be evaluated by setting the high-voltage generator to a typical voltage that will be used during the sensor characterization (e.g 300 V) and acquiring the AC-coupled output voltage. The output ripple is found to be predominantly contained inside the 50mV amplitude range as shown in figure 5.9.

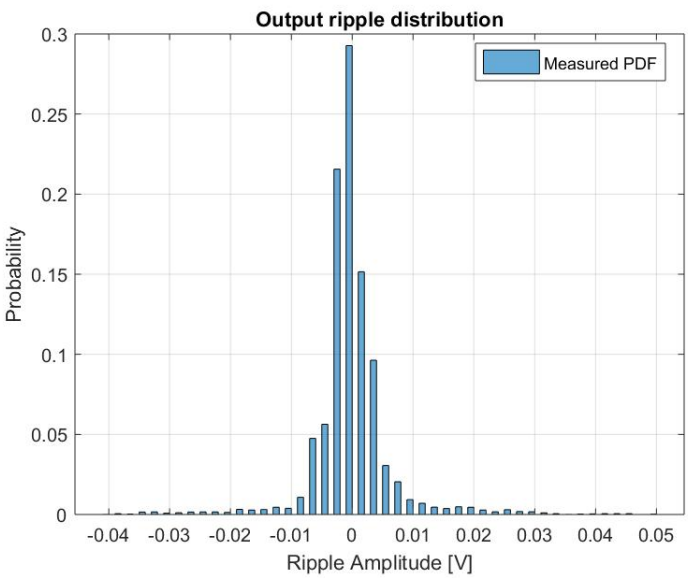


Figure 5.9 – **Probability Density Function (PDF) of the output ripple at a DC voltage of** 300 **Volts.** The output ripple is found to be predominantly contained inside the 50mV amplitude range. The PDF has been generated using 10000 measurement samples. The distribution has a **mean of zero Volt** (relative to the 300V DC) and a **standard deviation of 6.5 mV**.

The ripple spectrum is shown in figure 5.10. As it will be explained in the next chapters, a sine wave at frequencies above 500 Hz will be used for capacitance measurements. Figure 5.10 shows that there is only the effect of the noise floor at frequencies above 500 Hz. The effect of the ripple on the capacitance measurement can thus be ignored.

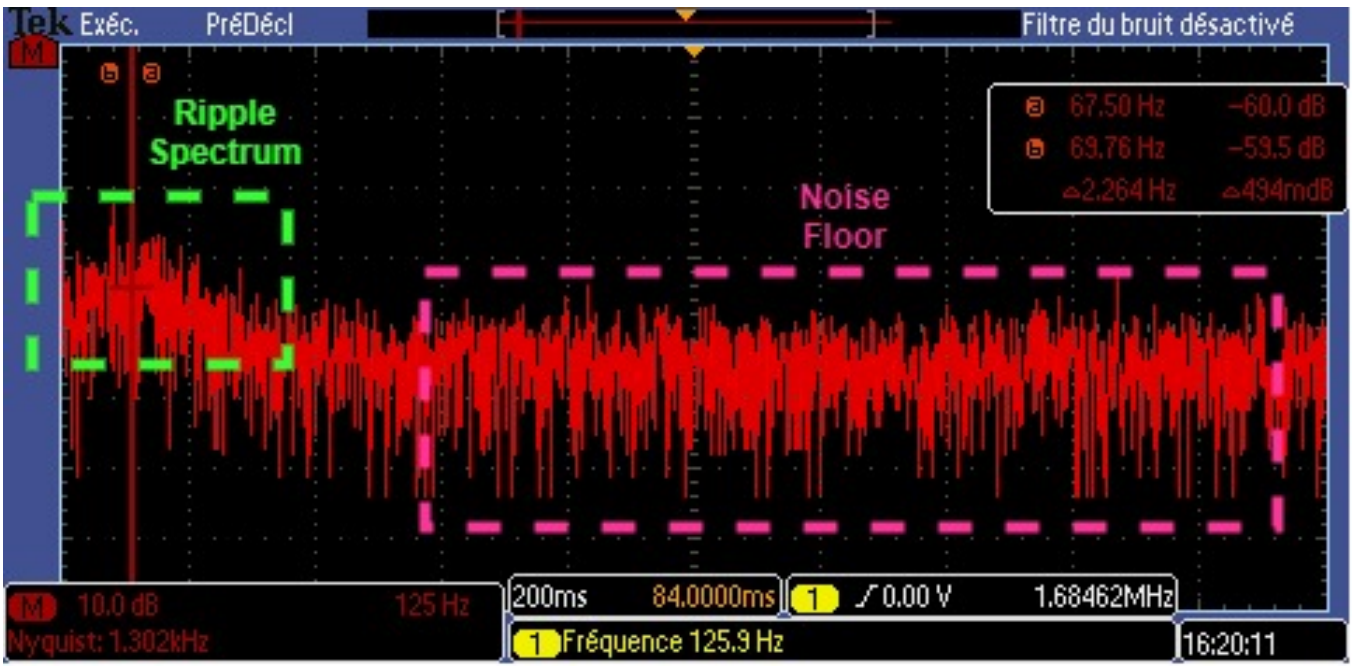


Figure 5.10 – Resulting **ripple spectrum** after the introduction of the output filter. **Horizontal scale:** 125Hz per division, **vertical scale:** 10dB per division.

The specifications on the ripple amplitude have thus been reached: the ripple amplitude is experimentally found to be around 50 **mV which is smaller than *the maximum tolerated ripple of*** 100 ***mV*** **imposed in the specifications.**

5.3 Conclusion

In this chapter, the design of the high-voltage generator that will be used to reverse-bias the Silicon sensors has been detailed. As the generator is digitally regulated, the voltage can be set by the external interface software through the Slow Control Board firmware. The PID coefficients have been derived. The low-ripple aspect of the generator has also been demonstrated and the initial specification on the ripple has been attained. This circuit will be used during I-V and C-V curve measurements. The reader will find the complete schematic of the high-voltage generator circuit in Appendix I.

Chapter 6
Design of the current measurement circuit

In order to measure I-V and C-V curves, current measurements must be done. In the case of I-V curves, the DC high-voltage is applied to a sensor to reverse-bias it and the DC leakage current is measured. In the case of C-V curve measurements, the sensor under test is reverse-biased and excited using a sinusoidal signal on top of the high-voltage line. In this latter case, the current must also be sampled to measure the amplitude of the resulting excitation current in order to derive the capacitance of the sensor.

This chapter presents the design of an isolated current measurement circuit that will be used to measure the leakage and excitation currents consumed by the sensor under test, which will enable I-V and C-V curve measurements.

6.1 Circuit Specifications

The current measurement is done at high-side (i.e. between the high-voltage supply and the sensor). Two ranges are required: $\pm 7\mu$A with resolution $<$ 6nA for the DC leakage current measurement and $\pm 50\mu$A with resolution $<$ 30nA for the AC excitation current measurement used during capacitance measurement.

The range specification for the DC leakage current was directly deduced from the sensor data-sheet (internal CMS document). The current range for the AC measurement is chosen knowing that the capacitance of the sensors without biasing is of the order of 50nF and the shunt resistor should be in the order of 10kΩ to achieve acceptable resolutions ($<$ 30nA) on the current measurement (this point will be detailed in section 6.2). The sinusoidal excitation will have a peak-to-peak amplitude of $\sim$ 1V and a frequency $\sim$ 1kHz. Using those orders of magnitude, the maximal current amplitude is derived in equation 6.1 (which is an over-estimation as the series resistor of the sensor has been ignored).

$$I_{max} = \frac{0.5V}{\sqrt{(\frac{1}{2\pi 1kHz 50nF})^2 + (10k\Omega)^2}} \sim 47\mu A \tag{6.1}$$

Equation 6.1 gives the current amplitude flowing in a series RC circuit for an excitation voltage amplitude of 0.5V at 1kHz. The capacitance is set to 50nF and the shunt resistor is set to 10kΩ. A range of 50μA is thus well suited.

6.1.1 Modification to the leakage current range specification

During the experimental validation of the SCB, only old Silicon sensors were available at the IIHE. Most of those sensors were consuming *less leakage current* than the 2S sensors. For this reason, the range specification for the leakage current has been reduced to $\pm 1.3\mu$A to reach a better resolution of $\sim$ 1nA. This tradeoff between range and resolution will be

detailed in the next section.

6.2 Circuit Design

Figure 6.1 shows the block diagram of the current measurement circuit.

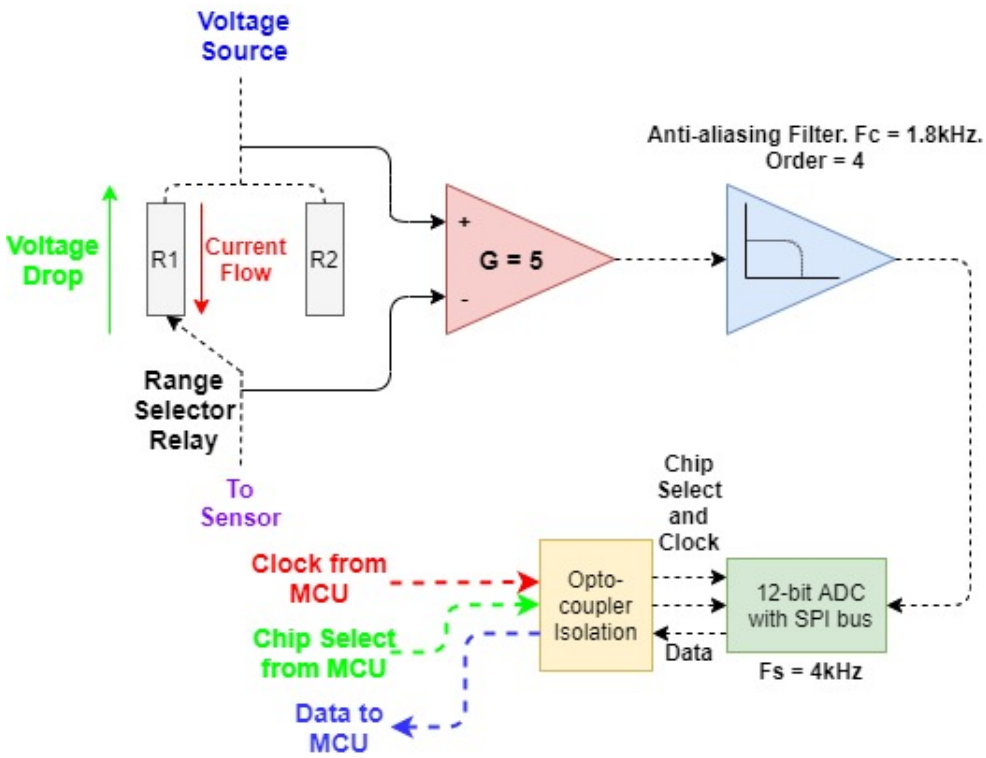


Figure 6.1 – Block diagram of the current measurement circuit

Two current ranges can be selected using the *range selector relay* by changing the shunt resistor used in the circuit. The voltage source (either DC high-voltage or AC sinusoidal voltage superimposed on top of the DC high-voltage) is connected to the high-side of the shunt resistor. The sensor is then connected to the low-side of the shunt resistor such that the consumed current induces a voltage drop across the shunt resistor.

A differential amplifier with gain $\times 5$ is then used to convert the differential voltage drop to a single-ended voltage signal. This signal is then passed to an anti-aliasing filter of order 4 with a cutoff frequency of 1.8kHz. The filtered signal is converted to the digital domain (SPI bus) by a 12-bit ADC. As the whole circuit operate at the high-voltage side, the SPI bus must be isolated with regard to the MCU using opto-couplers.

The MCU samples the current measurement at a rate of 4kHz using the *chip select* line. The SPI *clock* is also provided by the MCU. The data coming from the ADC is then read by the MCU. The current is thus sampled and stored for further processing.

Using this circuit gives rise to a *tradeoff* between current range and current resolution. Indeed, if the shunt resistance is made larger, the current measurement resolution

becomes finer but the voltage drop across the shunt resistor becomes larger which limits the range as the output of the differential amplifier is limited to ±2.5V (due to the ±2.5V power-rails), the amplifier will thus reach saturation at smaller voltage drops for larger shunt resistors.

The absolute best resolution on the measurement can be derived using equation 6.2, taking into account the maximum voltage span of the signal given to the ADC (2.5V−(−2.5)V = 5V), the bit width of the ADC (12-bit), the gain of the differential amplifier (×5) and the shunt resistor R.

$$\delta I = \frac{2.5 - (-2.5)}{4096} \frac{1}{5R} \tag{6.2}$$

The final parameters for the current measurement ranges are given in table 6.1.

Mode	**Shunt resistance**	**Range**	**absolute δI**
I-V range	300kΩ	±1.66μA	0.8nA
C-V range	10kΩ	±50μA	24.4nA

Table 6.1 – Parameters of the current measurement ranges.

During the design, the choice of filter order and cutoff frequency were derived by forcing the noise to fall below the quantization level of the ADC given by equation 6.3.

$$\delta q = \frac{5V}{4096} = 1.2mV \tag{6.3}$$

The high-voltage generator is by far the dominant noise source in the system, with a standard deviation of 6.5mV (see figure 5.9) and the *stop band* of the filter is chosen to be 2.5kHz in order to avoid aliasing of frequencies from 500Hz onward (as the sinusoidal excitation used to measure capacitance will be higher than 500Hz).

The anti-aliasing filter is built using two cascaded Butterworth filters of order 2 to provide a gain as constant as possible in the passband region. Figure 6.2 shows the anti-aliasing filter built around the Sallen-Key topology.

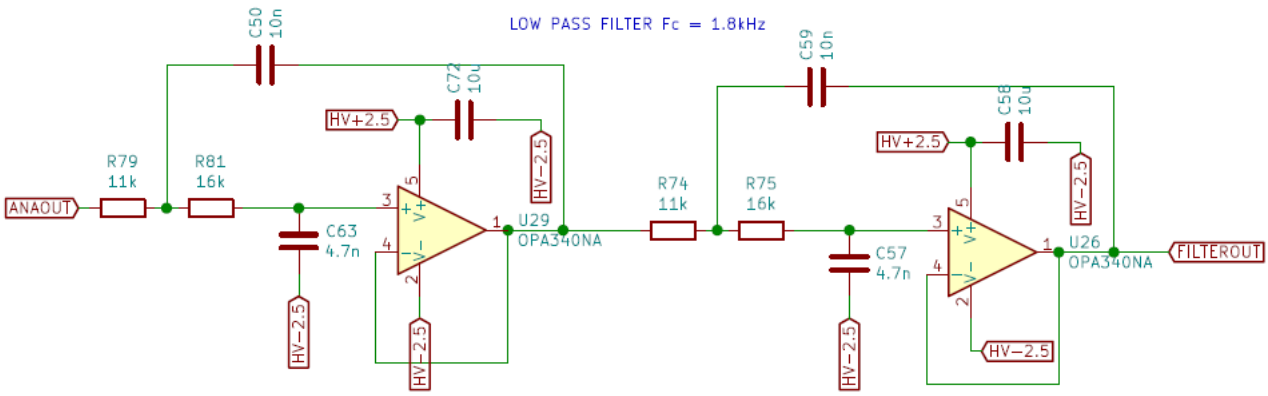


Figure 6.2 – **Anti-aliasing filter.**

Using SPICE simulation, the Bode diagrams of the filter have been generated (figure 6.3). The attenuation at 2.5kHz is found to be −15dB. A noise component z at this frequency with an amplitude of 6.5mV (standard deviation of high-voltage ripple) will be attenuated following equation 6.4.

$$z = \frac{0.0065V}{10^{\frac{15}{20}}} = 1.15mV \tag{6.4}$$

Thus, the noise contribution z falls below the quantization level δq which validates the design. It is still important to note that other sources of noise are also present such as the noise from the sine wave generator. Furthermore, the standard deviation of the high-voltage ripple has been solely considered here instead of the maximum amplitude of the noise. Nevertheless, the noise is strongly attenuated by the filter and averaging over the measurements will attenuate the effect of the noise even more.

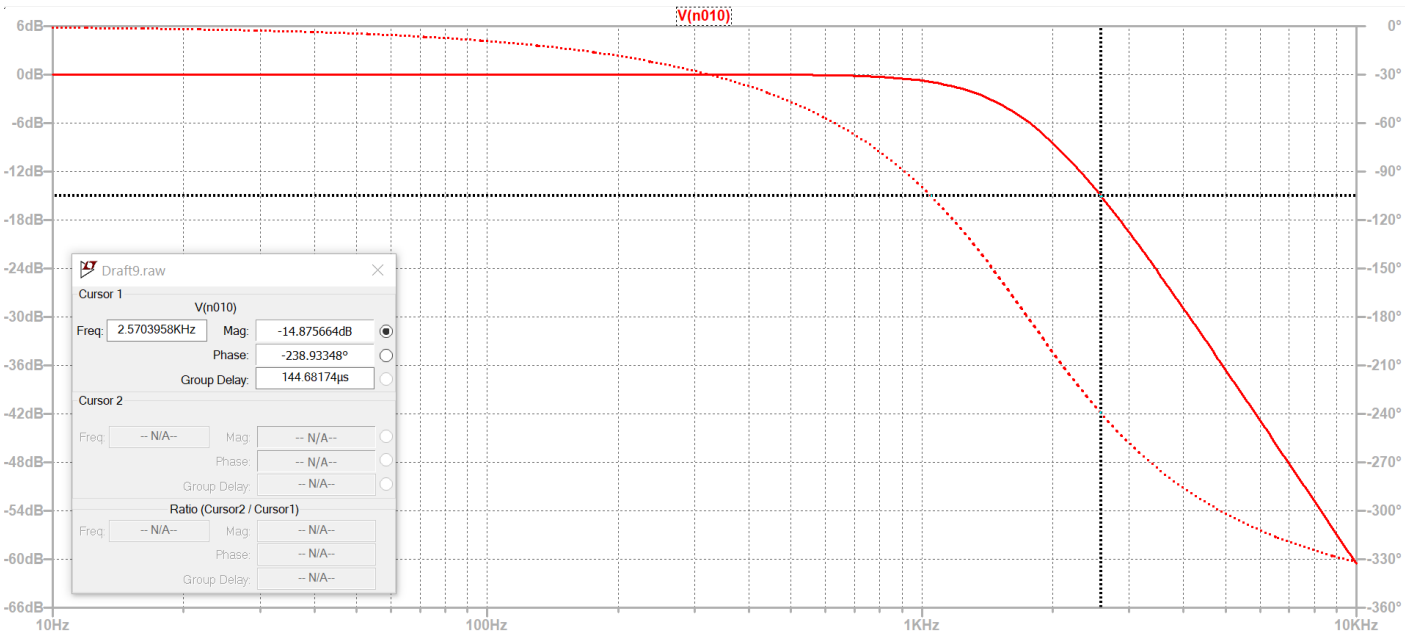


Figure 6.3 – Bode diagrams of the anti-aliasing filter.

For the DC current measurement, averaging over measurements will attenuate the effect of the ripple and noise. The reader will find the complete schematic of the current measurement circuit in Appendix I.

6.3 Estimation error on the leakage current measurement

After PCB tape-out and system validation, the standard deviation of the leakage current measurement has been estimated by acquiring the I-V curve of a very large resistor ($\sim$ 4000MΩ) by spanning a voltage range of $0 - 800$V. For each voltage step, the mean over 1024 current measurements has been computed. Then, the least-square-error line has been fitted to the measured I-V curve. The standard deviation of the leakage current estimation is found as the standard deviation of the error between the measured I-V curve and the fitted line. Figure 6.4 shows the measured I-V curve and the fitted line.

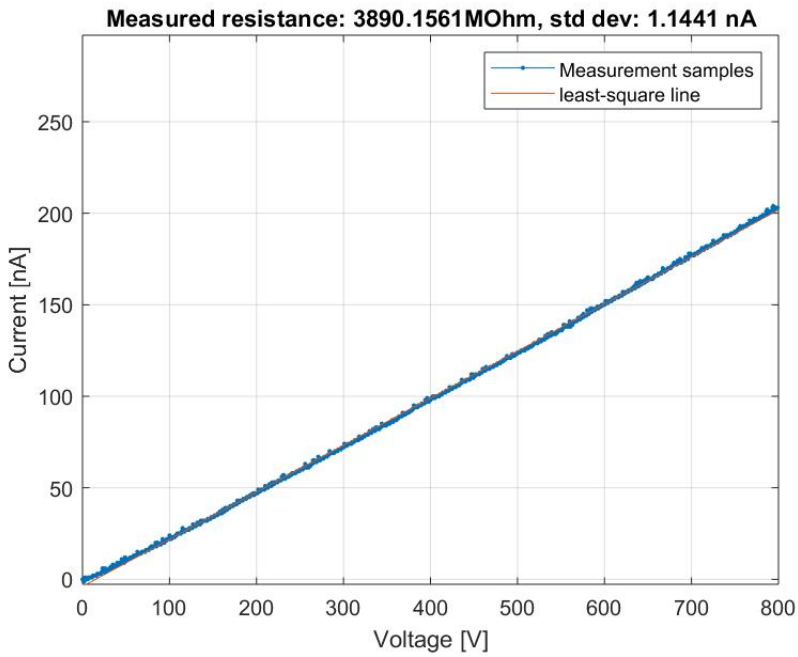


Figure 6.4 – I-V curve of a $\sim$ 4000MΩ resistor with least-square fitted line.

The standard deviation σ of the leakage current estimation is 1.14nA. The leakage current resolution can then be found using equation 6.5 [17] (see appendix C for a proof).

$$\sigma^2 = \frac{\delta q^2}{12} \tag{6.5}$$

The current measurement resolution δq is thus equal to $\sqrt{12}\sigma = 4$nA which is five times higher than the best achievable resolution of 0.8nA (see table 6.1). This experimental analysis holds for the leakage current measurement range but can be used to estimate the effective resolution of the AC current measurement used for capacitance estimation. Indeed, the resolution is expected to be five times higher than the best achievable resolution of 24.4nA. The **standard deviation on the capacitance estimate** using this circuit is discussed in the next chapter.

In practice, the proposed circuit was *totally capable of measuring I-V and C-V curves of real-world sensors* (see section 9.1.2) even if the precise specification on current measurement resolution was not exactly met. The maximal error of the capacitance estimation using this circuit was measured to be 0.32% on the specified capacitance range (see section 7.4) while a maximal error of 1% (given in the initial specifications) was already satisfying. This indicates that **the specification on AC current measurement resolution was stronger than needed**. The same can be said for the specification on DC current measurement as I-V curves with satisfying granularity can be acquired using the circuit (see section 9.1.2).

It is worth noting that by taking longer averaging over the current measurements, better resolutions are expected to be reached as the noise contribution is attenuated more and more (a mean over N samples will attenuate the noise power σ_z^2 as $\frac{\sigma_z^2}{N}$). This *measurement*

length parameter could be later changed in the firmware and software if needed.

Recalling section 6.1.1, **the specification on the leakage current measurement range was changed** to make the system capable of measuring so-called *phase-0* sensors (older generation of Silicon sensor), as the new 2S sensor were not available at the IIHE during the project. The original specification for leakage current measurement range can be easily met by changing back the leakage current shunt resistor from 300kΩ to a 71kΩ resistor.

6.4 Acquiring I-V curves

The I-V curve of a sensor is defined as the evolution of its leakage current in function of the reverse-bias voltage **at the sensor terminals**. The circuit described above measures the leakage current at high-side using a 300kΩ shunt resistor such that a significant voltage drop across the shunt resistor occurs due to the leakage current. Because of this voltage drop, the reverse-bias voltage at the terminals of the sensor is not exactly equal to the voltage imposed by the high-voltage generator (see figure 6.1).

During the I-V measurements, a sequence of leakage current $\underline{I} = [I_1, ..., I_N]$ is acquired for a sequence of voltages $\underline{V} = [V_1, ..., V_N]$ generated by the high-voltage circuit. The voltage drop across the shunt resistor will be compensated after the current acquisition by subtracting the voltage drop across the shunt from the voltage sequence $\underline{V}$ (equation 6.6).

$$\underline{V}_{comp} = \underline{V} - 300k\Omega \times \underline{I} \tag{6.6}$$

By doing so, the sequence of leakage current $\underline{I}$ will correctly correspond to the sequence of reverse-bias voltage **at the sensor terminals** $\underline{V}_{comp}$ such that correct I-V curves will be displayed by plotting $\underline{I}$ in function of $\underline{V}_{comp}$.

6.5 Conclusion

In this chapter, the specifications for the current measurement circuit have been motivated, the circuit design has been detailed and the effective resolutions for the leakage current and the AC current measurement ranges have been discussed by experimentally acquiring an I-V curve for a 4000MΩ resistor. This current measurement circuit will be used during I-C and C-V curve acquisition.

Chapter 7
Design of the capacitance measurement circuit

In order to estimate the full-depletion voltage of the sensors under test, an isolated capacitance measurement circuit must be designed. First, the sensors under test will be modelled. Then, using this model, a capacitance measurement circuit will be designed. The theoretical and experimental estimation errors will then be discussed and compared.

7.1 Modelling of the device under test

In order to optimize the design of the capacitance measurement circuit, it is of interest to model the device under test (DUT). Table 7.1 shows the electrical parameters of the 2S sensor modules at full depletion.

Number of strips	Active width w	Active length l	Active height h	Bias resistor per strip R_{bias}
2032	91440 μm	100548 μm	290 μm	1.5 MΩ $\pm$ 0.5MΩ

Table 7.1 – Electrical parameters of the 2S sensor modules.

An order of magnitude for the equivalent capacitance C_{eq} of the sensor can be found using the planar capacitance model (equation 7.1).

$$C_{eq} \approx 2032 \times \frac{\epsilon_r \epsilon_0 w l}{h} = 3.28nF \tag{7.1}$$

where ϵ_r is the relative permittivity of Silicon.

As C_{eq} is inversely proportional to the square root of the reverse-bias voltage [5], the value of C_{eq} (found at full depletion and computed in equation 7.1) represents the **minimal** capacitance that will be measured on the C-V curves. Therefore, the capacitance measurement circuit must be able to measure capacitance values as low as the one found in equation 7.1.

Each Silicon strip is connected to a polysilicon bias resistor. An equivalent bias resistance R_{eq} for the whole sensor, formed by connecting in parallel all the Silicon strips can be derived (equation 7.2).

$$R_{eq} \approx \frac{R_{bias}}{2032} = 738.2\Omega \pm 246.1\Omega \tag{7.2}$$

Furthermore, each Silicon strip is subject to a leakage current. A maximum leakage current of 7.25μA for the whole sensor is specified at a reverse-bias voltage of 600 V in the sensor data-sheet (available during the project). This leakage current will be modelled by a leakage resistor R_{leak} in parallel with C_{eq}.

As explained in the previous chapter, the current measurement circuit has two ranges: one for leakage current measurements and another one for measuring currents of higher amplitudes. This second range will be used to measure the excitation current resulting from the sinusoidal voltage signal that will be applied to the DUT during capacitance measurement. The shunt resistor of this current measurement range (10 kΩ) must be included in the *equivalent circuit* that will be measured.

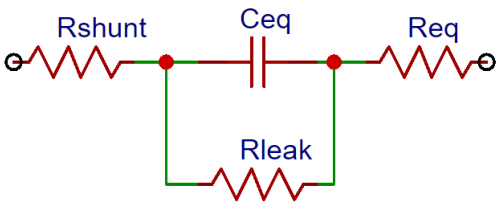


Figure 7.1 – **Equivalent circuit.** C_{eq}, R_{eq} and R_{leak} model the DUT and R_{shunt} denotes the shunt resistor used in the current measurement circuit.

It is of interest to know the order of magnitude of R_{leak} in function of the reverse bias voltage. In first-order approximation, the leakage current is proportional to the square root of the reverse bias voltage V_{bias} [5]. Using the fact that a total maximal leakage current I_{lm} of 7.25μA is expected for a reverse bias voltage of 600V, R_{leak} can be found as the following:

$$R_{leak} = \frac{V_{bias}}{\frac{I_{lm}}{\sqrt{600}}\sqrt{V_{bias}}} - R_{eq} \tag{7.3}$$

Using equation 7.3, the first-order evolution of R_{leak} in function of V_{bias} can be found in figure 7.2.

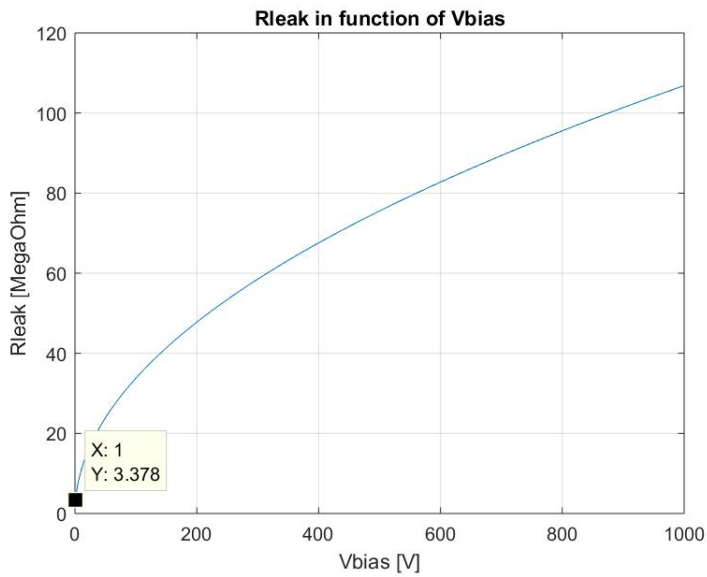


Figure 7.2 – **Evolution of R_{leak} in function of V_{bias}.** Using the first-order approximation $I_{leak} \sim \sqrt{V_{bias}}$.

Figure 7.2 shows that $R_{leak} > 1M\Omega$. When feeding a sine wave excitation to the equivalent circuit of figure 7.1, the effect of R_{leak} could be ignored if the impedance of C_{eq} is smaller than a worst-case scenario of $R_{leak} \sim 1M\Omega$. This is depicted in equation 7.4.

$$\frac{1}{2\pi f_e C} << 10^6\Omega \tag{7.4}$$

Replacing the lowest expected value of C_{eq} (3.28nF) in equation 7.4, a condition on the excitation frequency f_e is found (equation 7.5).

$$f_e >> 50Hz \tag{7.5}$$

It must be noted that equation 7.5 depicts a worse-case scenario. Indeed, the lowest expected value of C_{eq} (3.28nF) is obtained at full depletion, where $R_{leak} \sim 10$ MΩ, making the presence of R_{leak} **even more insignificant**. An excitation frequency of at least one order of magnitude higher than equation 7.5 can be safely used, leading to the simplified equivalent circuit of figure 7.3.

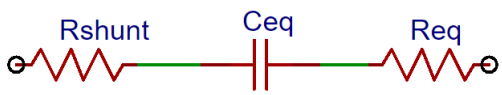


Figure 7.3 – **Simplified equivalent circuit.**

The design of the capacitance measurement circuit will be done around the simplified model shown in figure 7.3 with the constraint that the excitation frequency used to characterize the DUT will need to satisfy equation 7.5.

7.2 Capacitance measurement strategy

As said earlier, the capacitance of the sensors will be measured by reverse-biasing the sensors and feeding a sinusoidal voltage on top of it. As the equivalent circuit is composed of a resistor in series with a capacitor (figure 7.3), measuring the amplitude and the phase-shift of the resulting excitation current (with regard to the sinusoidal excitation voltage) will enable the measurement of C_{eq}. Figure 7.5 shows the measurement circuit topology.

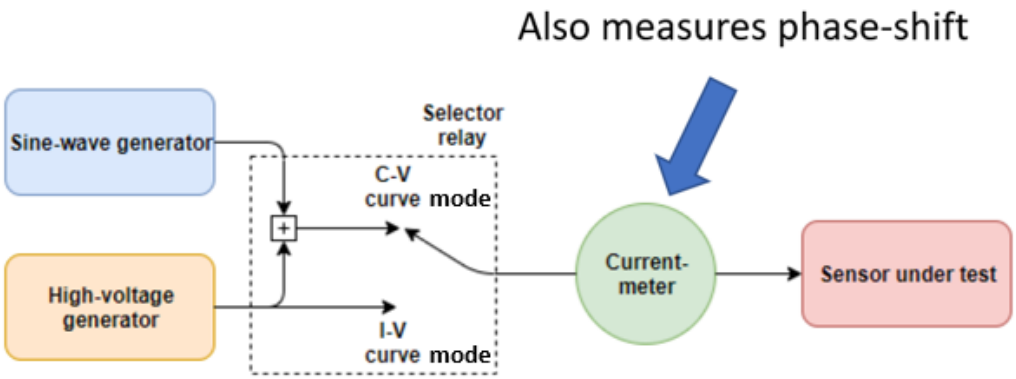


Figure 7.4 – **Measurement circuit block diagram.** When measuring capacitance, the C-V curve mode is selected. The Sensor under test is reverse-biased by the high-voltage generator and is excited by a sinusoidal voltage signal coupled on top of the high-voltage line. Then, a high-side current and phase-shift measurement circuit is used to derive the value of the sensor capacitance. **The phase-shift is measured between the resulting excitation current and the input excitation voltage.**

Equation 7.6 shows the relation between the resulting excitation current and the excitation voltage. $V(j\omega)$ and $I(j\omega)$ respectively denote the Fourier transform of the excitation voltage and the Fourier transform of the resulting excitation current.

$$I(j\omega) = \frac{j\omega C_{eq}}{j\omega(R_{shunt} + R_{eq})C_{eq} + 1} V(j\omega) \tag{7.6}$$

Using equation 7.6, the phase-shift and amplitude of the excitation current can be derived (equation 7.7 and 7.8).

$$\angle I(j\omega) = \frac{\pi}{2} - \arctan(\omega(R_{shunt} + R_{eq})C_{eq}) \tag{7.7}$$

$$|I(j\omega)| = \frac{|V(j\omega)|\omega C_{eq}}{\sqrt{\omega^2(R_{shunt} + R_{eq})^2 C_{eq}^2 + 1}} \tag{7.8}$$

Next, saturation of the current amplitude measurement circuit must be avoided during the measurements (range of $\pm 50\mu$A). Figure 7.5 shows the current amplitude in function of the capacitance to measure for different excitation frequencies (equation 7.8). The peak-to-peak amplitude of the excitation sine wave is set to 1V.

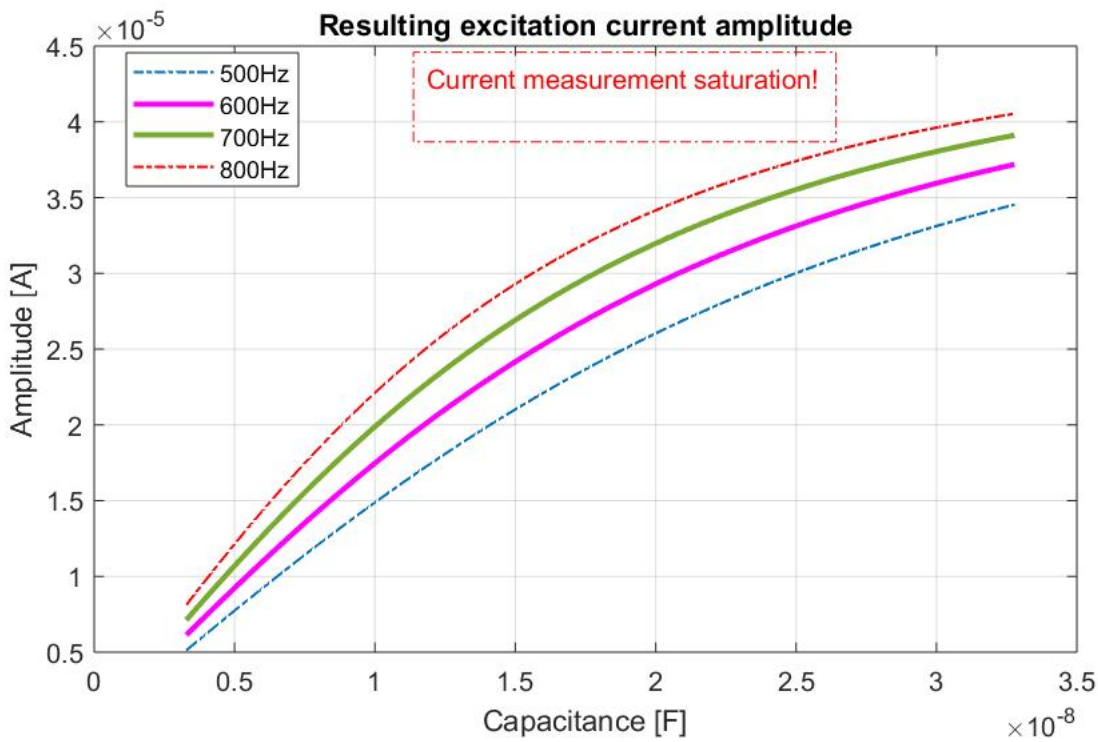


Figure 7.5 – **Current amplitude in function of the capacitance to measure.** Excitation voltage amplitude of 1 V_{p-p}.

Figure 7.5 shows that the current amplitude measurement circuit can be close to saturation at frequencies above 800 Hz. Thus, excitation frequencies from 500 Hz to 800 Hz must be used during measurements in order to avoid saturation of the current-meter, while respecting equation 7.5. The final parameters for the sinusoidal excitation are given by table 7.2.

Peak-to-peak amplitude	Frequency f_e
1 V	500-800 Hz

Table 7.2 – Sinusoidal excitation parameters

In practice, a sinusoidal excitation (with frequency of 600Hz) will be generated by an external function generator coupled to the high-voltage generated on the SCB using the circuit of figure 7.6. HV0, HV-2.5 and HV+2.5 respectively denote the high-voltage line and the isolated ±2.5V source coupled to HV0 (generated on the SCB). The input sine wave from the signal generator is first connected to an isolation transformer to avoid shorting the high-voltage line to the common ground reference (GNDREF). On the secondary side, one tap of the transformer is connected to the high-voltage line and the other one is connected to a voltage follower which will remove the series inductance of the transformer from the capacitance measurement circuit. The SINE output is then fed to the sensor through the current-meter to measure sensor capacitance.

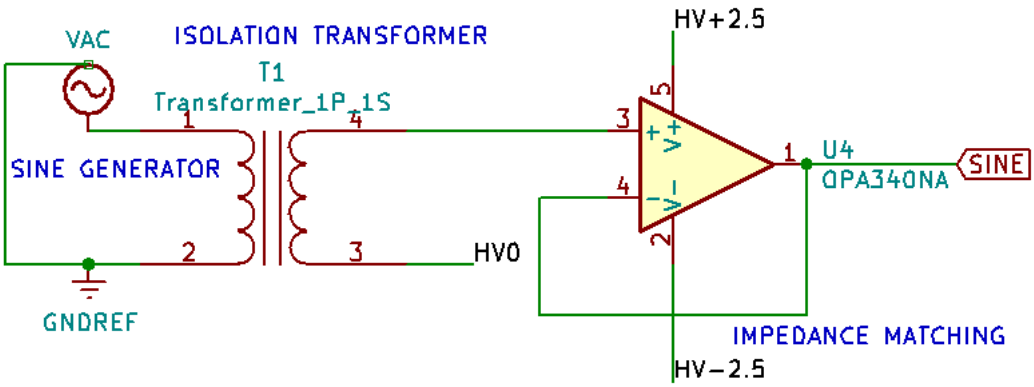


Figure 7.6 – Sine wave coupling circuit.

7.3 Design of a phase-shift and frequency measurement circuit

As stated in the previous section, the excitation sine wave will be generated by a function generator coupled to an isolation transformer. The induced excitation current will present a phase-shift that must be measured. Additionally, the excitation frequency will also be measured to make the capacitance calculation more precise.

The proposed circuit is shown in figures 7.7 and 7.8. The excitation sine wave and the resulting sinusoidal excitation current will first be converted to binary pulse signals using two comparators with a threshold at ground level. When the sine waves have positive values, the outputs of the comparators will become high.

As the excitation sine wave will be generated on top of the high-voltage line, the comparators must be isolated using two opto-couplers. The binary pulse trains coming from the opto-couplers will then be given as input to the micro-controller. Using an integrated timer in capture-compare mode, the frequency of the pulse trains (corresponding to the frequency of the sine waves) and the phase-shift between the pulse trains (corresponding to the phase-shift between the two sine waves) will be retrieved.

Figure 7.7 shows the isolated sine wave to pulse converter circuit, implemented on the PCB. Additional care has been given to the power supply decoupling of the comparators and opto-couplers in order to generate sharp pulses. The analog ground level (*AGND* on the schematic) corresponds to the voltage level of the high-voltage line while *VDDA* and *GNDD* are generated by an isolated 5V regulator and corresponds to the ±2.5V rails. Two rail-to-rail op-amps (U31 and U32) have been used as comparators. The circuit is isolated using the two opto-couplers (U34 and U35).

The two outputs of the isolated sine wave to pulse converter circuit (*Excpulse* and *Ipulse*) are then given as input to the circuit shown in figure 7.8, implemented inside the micro-controller. If the frequency must be measured, the multiplexer routes the pulse

signal corresponding to the excitation sine wave to the *trigger* and *capture* inputs of the timer. Else, if the phase-shift needs to be measured, the pulse signal corresponding to the resulting excitation current is routed to the *trigger* input. By triggering and capturing on the rising edges of the signals, the frequency and the phase shift can be found. When a capture has occurred, an interrupt routine is fired to read the timer register and to reset it for the next acquisition.

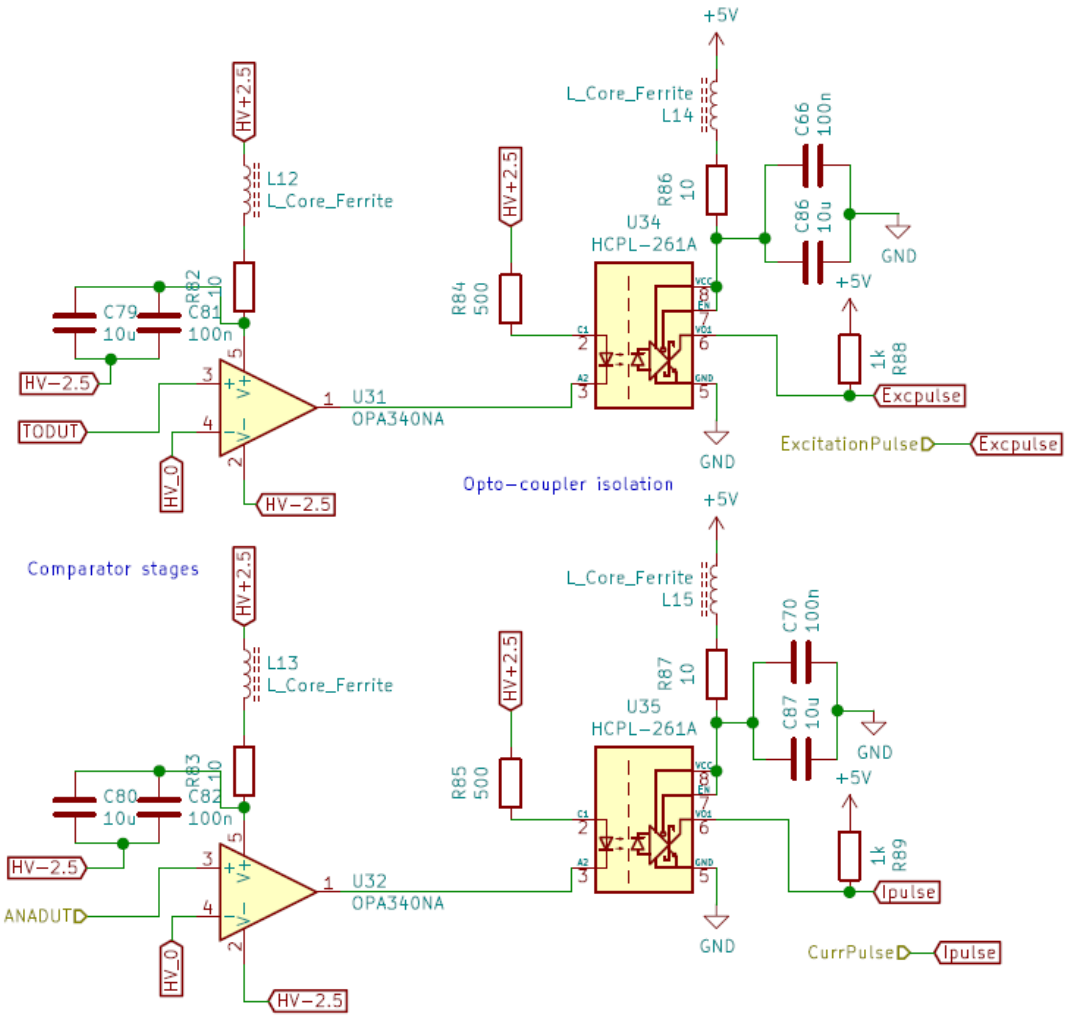


Figure 7.7 – **Isolated sine wave to pulse converter circuit.** *TODUT* and *ANADUT* are respectively the excitation and current sine waves. *Excpulse* and *Ipulse* are the corresponding pulse signals given as inputs to the PSOC micro-controller.

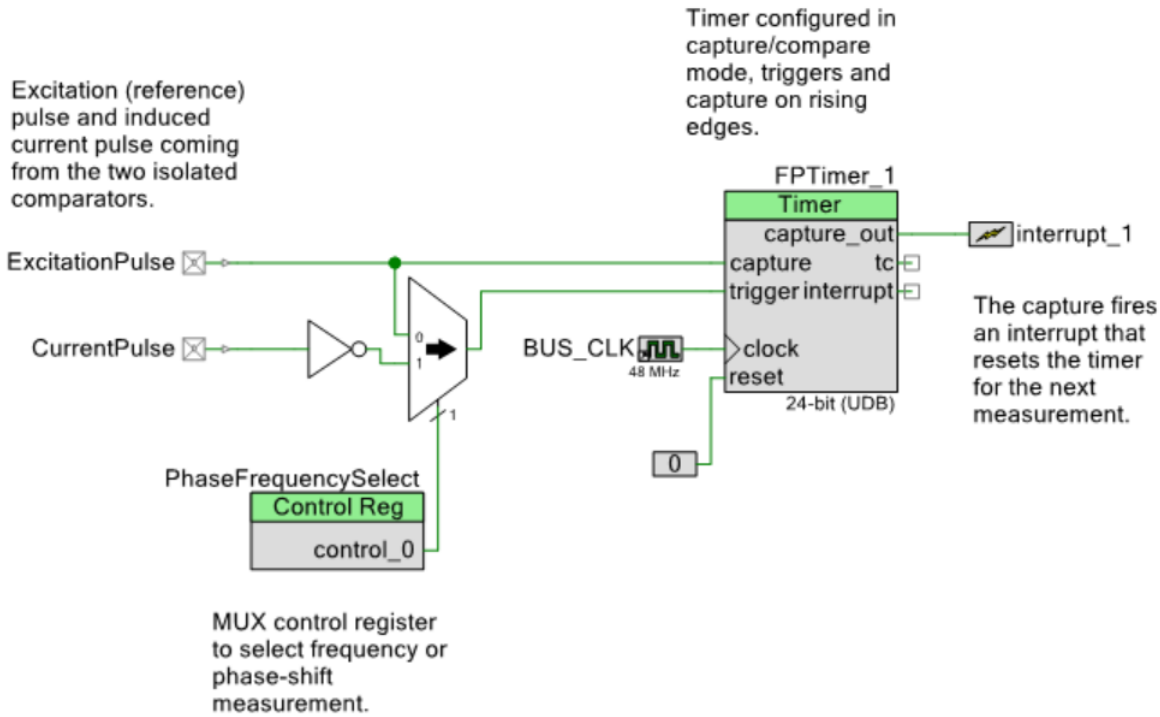


Figure 7.8 – Frequency and phase-shift measurement circuit.

7.4 Estimation error on the capacitance measurement

Using the measurement parameters and circuits proposed in the previous sections, the capacitance estimation error can be evaluated by back-propagating the uncertainties on the phase-shift and current measurements. By re-arranging equations 7.7 and 7.8, equation 7.9 is derived. ϕ denotes $\angle I(j\omega)$ and I denotes $|I(j\omega)|$

$$C(I,\phi) = \frac{I\sqrt{\cot^2\phi + 1}}{\omega V} \tag{7.9}$$

The error on the capacitance estimate $\hat{C}$ is derived using equation 7.10.

$$\delta\hat{C} = \frac{\partial C}{\partial \phi}|_{(I_0,\phi_0)}\delta\phi + \frac{\partial C}{\partial I}|_{(I_0,\phi_0)}\delta I + \frac{\partial^2 C}{\partial\phi\partial I}|_{(I_0,\phi_0)}\delta\phi\delta I \tag{7.10}$$

By replacing $C(I,\phi)$ (equation 7.9) in equation 7.10, the expression for $\delta\hat{C}$ is derived (equation 7.11).

$$\delta\hat{C} = -\frac{I\cot\phi}{\omega V\sin^2\phi\sqrt{\cot^2\phi+1}}\delta\phi + \frac{\sqrt{\cot^2\phi+1}}{\omega V}\delta I - \frac{\cot\phi}{\omega V\sin^2\phi\sqrt{\cot^2\phi+1}}\delta\phi\delta I \tag{7.11}$$

$\delta\phi$ is derived using the micro-controller timer parameters. The timer period is set to 1.875ms and the number of counts during the period is 90000 which leads to a time estimation uncertainty of $\delta\tau = \frac{0.001875}{90000} = 20.83$ns. $\delta\phi$ is then found using equation 7.12 (where $f_e = 800$Hz).

$$\delta\phi = 2\pi f_e \delta\tau = 0.00104 rad \tag{7.12}$$

The uncertainty on the current measurement was derived in the previous chapter ($\delta I = 24.4$nA). By introducing $\pm\delta\phi$ and $\pm\delta I$ in equation 7.11, four curves showing $\delta\hat{C}$ in function of C (the ground truth capacitance value) are found (discontinued blue and orange lines, continued yellow and green lines in figure 7.9).

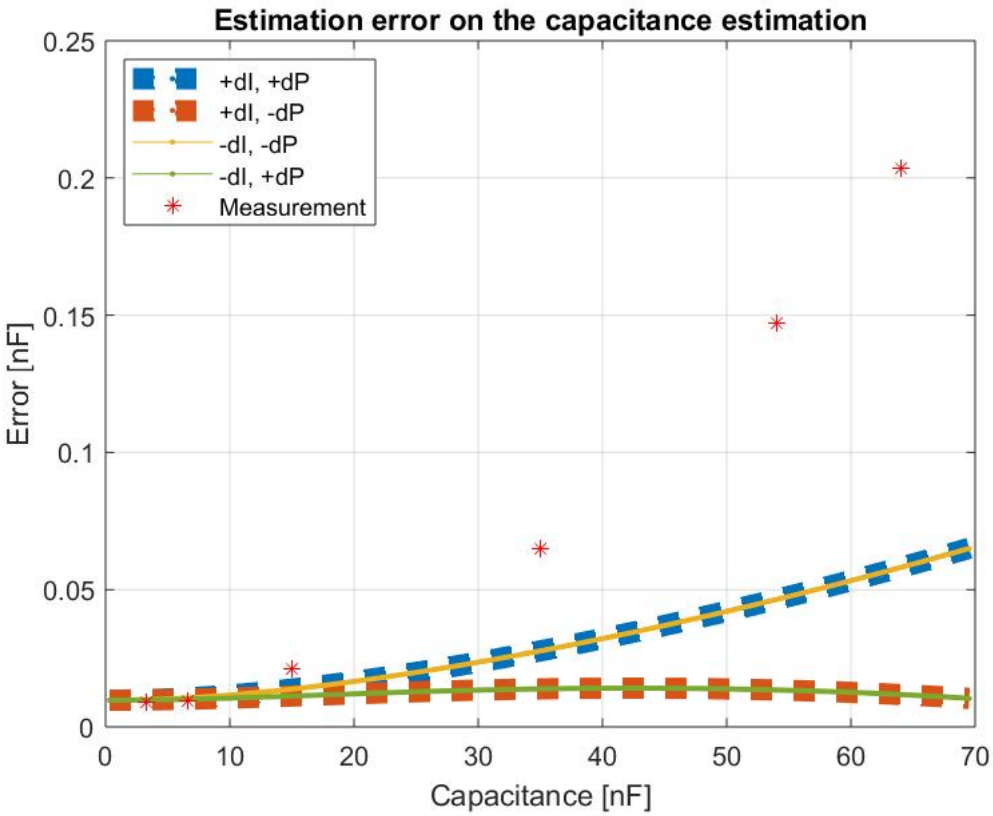


Figure 7.9 – **Estimation error on the capacitance measurement.**

The estimation error simulation shows that a theoretical maximum error of 70pF is expected on the measurement range. This simulation validated the proposed circuits for tape-out. **After PCB tape-out and system validation**, the *real-world* standard deviation of the capacitance estimation using 40 measurements on 6 dummy capacitors has been measured (red stars in figure 7.9). Those measurements show that the simulation is accurate for lower capacitance values (red stars are close to simulation curves) while for higher capacitance values, the simulation is still close to the measured order of magnitude on the full capacitance range even if the deviation becomes significant. **Using the measurements, the maximum relative estimation error for the capacitance measurement has been found to be** 0.32%**, the desired specification (*capacitance estimation error* < 1 %) has thus been attained.**

7.5 Conclusion

In this chapter, a model for the sensors under test has been derived, the approach behind the capacitance measurement circuit has also been detailed. The proposed circuit has been approved by simulating the error on the capacitance estimate in function of the capacitance to measure. After PCB tape-out, the estimation error has been measured experimentally and was found to be of the same order of magnitude than the simulation, giving a maximum relative error of 0.32% on the capacitance estimate. The desired specification has thus been reached. The reader will find the complete schematic of the capacitance measurement circuit in Appendix I.

Chapter 8

Processing cues used within the interface software

In this section, the two most important data processing cues used within the interface software will be presented, namely *excitation current measurement* (used for C-V curve measurement) and *full-depletion voltage identification*.

It should be noted that a plethora of other processing and control schemes have been implemented in the C++ core of the interface software and in the Python user interface code such as *hand-shake* communication between the interface software and the SCB, *dew point temperature* calculation, capacitance estimation and so-on.

8.1 Excitation current amplitude measurement via spectral analysis

In order to derive the capacitance of the depleted sensors, the excitation current resulting from the sinusoidal excitation voltage superimposed on the high-voltage line must be measured with optimum *signal-to-noise ratio* (SNR).

After the acquisition of the sinusoidal excitation current by the SCB, 1024 current samples are sent to the interface software. The interface software must then be able to retrieve the amplitude of this sinusoidal current. As the excitation current amplitude is in the order of *micro-Amps*, a significant noise contribution is expected on the measurements making the precise acquisition of the amplitude by the mean of a simple *maximum-minimum tracking* algorithm unreliable.

Thus, *spectral analysis* has been used to de-correlate as more as possible the excitation current amplitude measurement from the noise. Indeed, the acquired signal in the time-domain is dense while its representation in the frequency domain is sparse. An *N-point* spectral analysis (N-point DFT) will thus provide a *processing gain* of at most N on the SNR during measurement (see figure 5.10). The spectrum of the acquired excitation current signal is generated using a 1024-point FFT algorithm [18] with a *Blackman* window as a single-tone is expected [19]. Figure 8.1 shows a spectrum generated by the interface software during a capacitance acquisition on an older generation of particle tracking sensor.

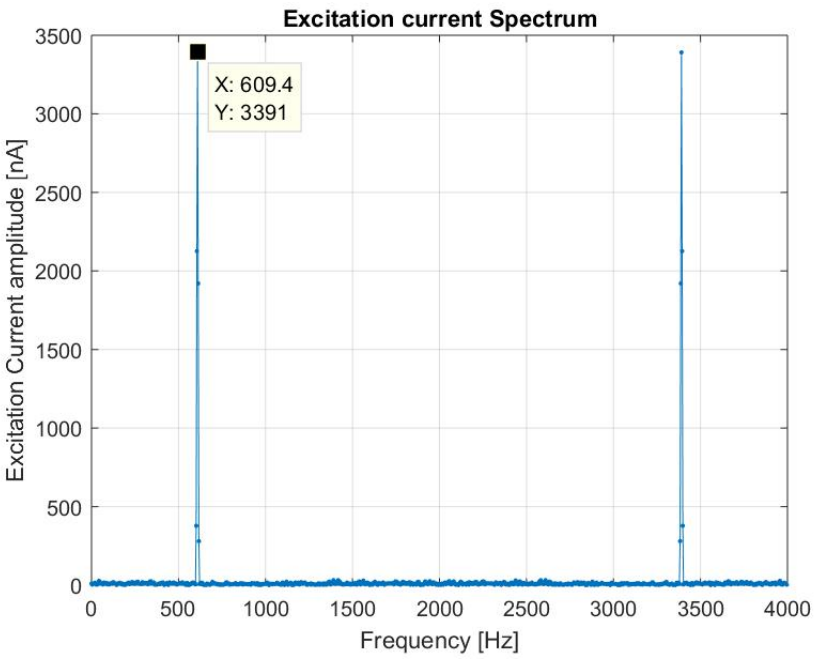


Figure 8.1 – **Excitation Current Spectral amplitude plot.** This spectrum has been generated by the interface software during a capacitance acquisition on an older *phase-0* sensor.

In figure 8.1, it is possible to remark the strong peak at the frequency of 609Hz due to the sine wave excitation. As the excitation frequency is measured through the use of the *frequency and phase-shift measurement circuit* explained in the previous chapter, it is possible to localise the sine wave component in the generated spectrum (independently of the spectrum itself) and to derive its amplitude.

The spectral amplitude $S[k]$ can be written as follows [20].

$$S[k] = |\frac{1}{N}\sum_{n=0}^{N-1} w[n].s[n]e^{-j2\pi\frac{nk}{N}}| \tag{8.1}$$

Where N is the number of samples (1024 in this case), $w[n]$ is the Blackman window and $s[n]$ is the acquired excitation current.

In order to derive the sine wave amplitude, the energy E_s of the frequency band around the measured frequency k_0 is calculated using equation 8.2.

$$E_s = 2\sum_{k=k_0-\delta}^{k_0+\delta} \tilde{S}^2[k] \tag{8.2}$$

Where δ defines the spread of the summation (set to 2) to take into account the spread of the peak imposed by the loss of frequency resolution due to the use of the Blackman window [19] and $\tilde{S}[k]$ is defined by equation 8.3 to compensate for the attenuation imposed by the Blackman window [21].

$$\tilde{S}[k] = \frac{N}{\sum_{n=0}^{N-1} w[n]} S[k] \tag{8.3}$$

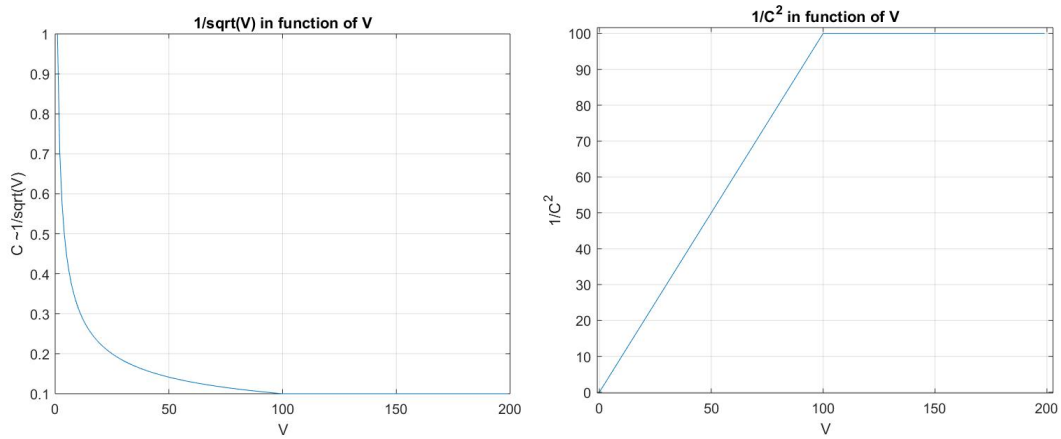
The amplitude A of the sine wave is finally derived using equation 8.4, by definition of the sine wave energy.

$$A = \sqrt{2E_s} \tag{8.4}$$

The interested reader will find a discussion on windowing in **appendix A** and a discussion on the processing gain provided by the DFT in **appendix B**.

8.2 Full-depletion voltage identification

The *full-depletion voltage* is defined as the minimum reverse-bias voltage for which the sensor has reached full depletion (the active area of the sensor is the widest possible). The full-depletion voltages can be identified by measuring the C-V curve of the sensors. As the sensor capacitance follows equation 3.5, the C-V curve is expected to reach a plateau where full depletion is attained. In practice, the $\frac{1}{C^2}$ *in function of* V curve will be preferred as it will linearize the graphs in their $C \sim \frac{1}{\sqrt{V}}$ region (before the plateau). For the sake of clarity, figure 8.2a shows a **toy example** of a C-V curve with its $\frac{1}{C^2}$ *in function of* V representation (figure 8.2b) where the linearized region appears.



(a) A toy example C-V curve **with plateau**. (b) A toy example $\frac{1}{C^2}$ in function V representation.

Figure 8.2

The full-depletion voltage is found by fitting *a line* to the linearly increasing region and *another line* on the plateau and by taking their *intersection*. The line fitting for the plateau is done by taking the mean over the plateau samples. For the linearly increasing region, the line fitting is done using *least squares*, a linear model of the form $\frac{1}{C^2} = aV + b$ is learned using equation 8.5 [22] (proof given in **appendix D**) where the matrices A and C are defined in equation 8.6 and 8.7 (V_1 to V_n denote the voltage steps of the linear region and C_1 to C_n denotes the corresponding capacitance measurements).

$$\begin{bmatrix} a \\ b \end{bmatrix} = (A^t A)^{-1} A^t C \tag{8.5}$$

$$A = \begin{bmatrix} V_1 & 1 \\ . & . \\ . & . \\ . & . \\ V_n & 1 \end{bmatrix} \tag{8.6}$$

$$C = \begin{bmatrix} \frac{1}{C_1^2} \\ . \\ . \\ . \\ \frac{1}{C_n^2} \end{bmatrix} \tag{8.7}$$

Figure 8.3 shows the application of *the full-depletion voltage estimation algorithm* on a CMS *phase-0* Silicon sensor measurement using the system built during this project.

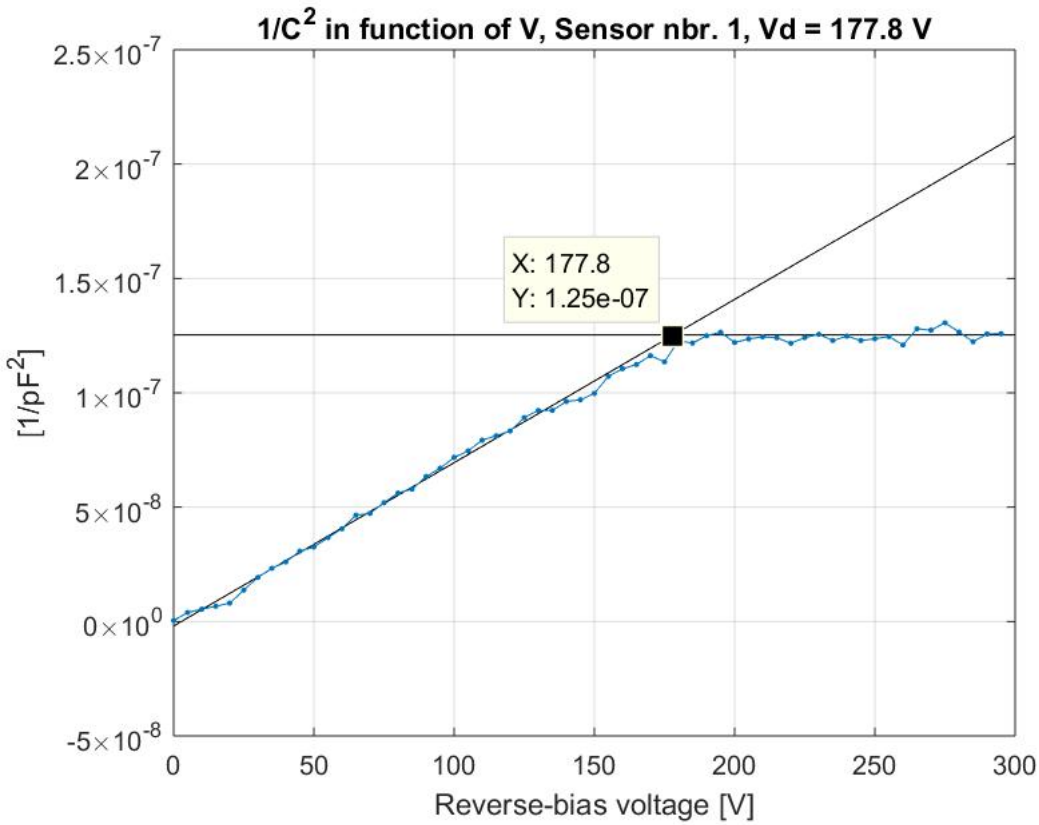


Figure 8.3 – **Full-depletion voltage estimation of a Silicon sensor**. The plateau is fitted by its average value and the linearly increasing region is fitted using *least squares regression*. The intersection of the two lines is the estimate of the full-depletion voltage of the sensor.

In the example of figure 8.3, the full-depletion voltage is estimated to be 177.8V. The method described above will also be used to estimate the full-depletion voltage in all the measurements shown in the next chapter.

8.3 Conclusion

In this chapter, the algorithms behind *excitation current measurement* and *full-depletion voltage identification* have been detailed. Measuring in the frequency domain has been introduced in order to provide an additional processing gain on the SNR during current measurements and the $\frac{1}{C^2}$ *in function* V representation has been introduced for full-depletion voltage estimation. Those techniques will be used during the measurements described in the next chapter.

Chapter 9
Experimental validation of the system

9.1 *Phase-0* tracking sensor characterization

In this section, Silicon sensors found on previous generation CMS tracker modules are characterized by generating their C-V and I-V curves.

9.1.1 Experimental set-up

A general view of the experimental set-up for the *Phase-0* tracking sensor characterization is shown in figure 9.1.

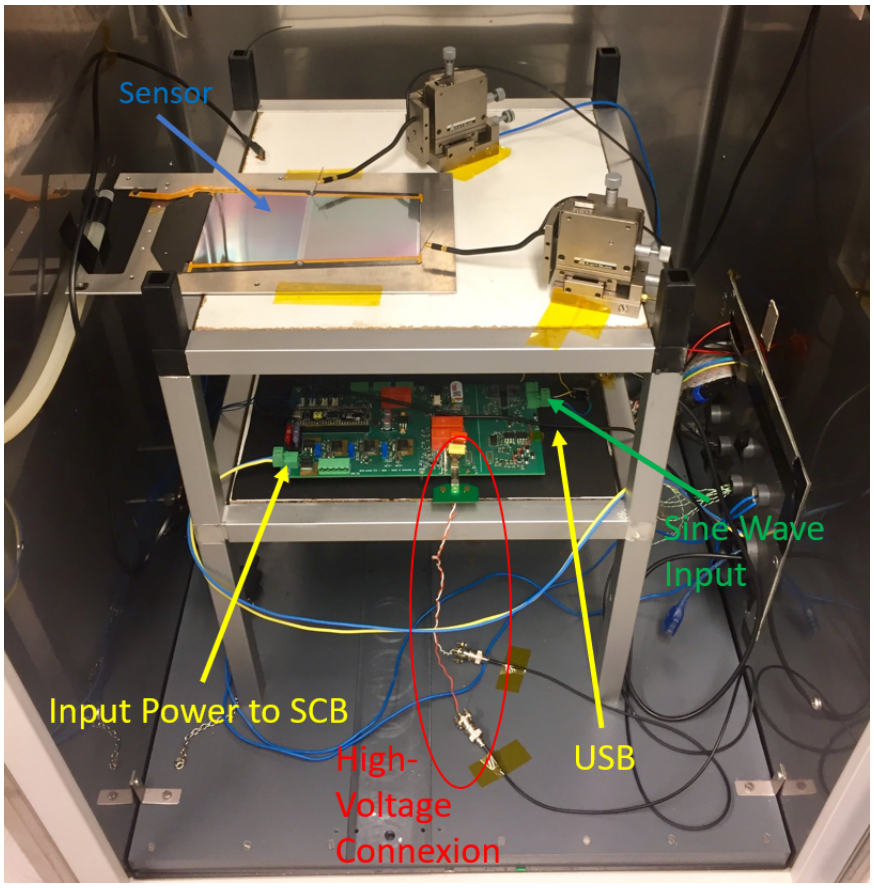


Figure 9.1 – **Vue of the experimental set-up** The SCB is connected to the sensor through its high-voltage output port. The power supply and function generator used to generate the sine waves are placed outside the fridge.

Figure 9.2 shows the electrical connections to the tracker sensor using a pair of *KarlSuss PH120 micrometer probe-heads* with the associated *KarlSuss* needles (circled in green on

the picture). The two environmental sensors for humidity and temperature acquisition can also be seen in figure 9.2 (circled in blue).

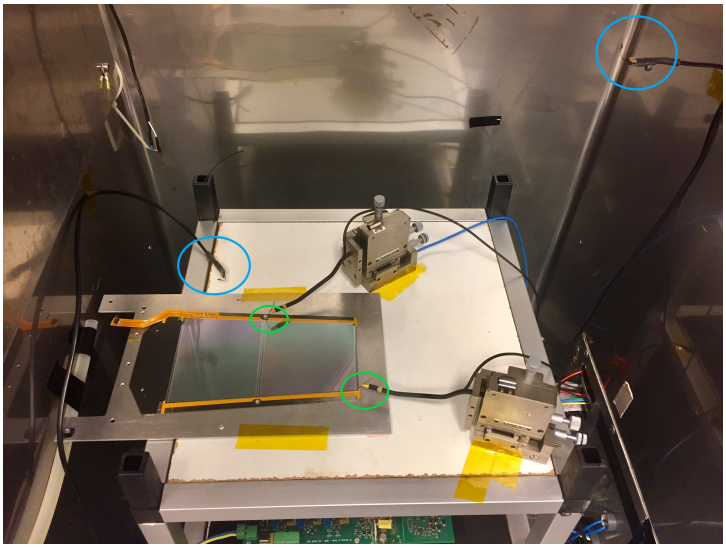
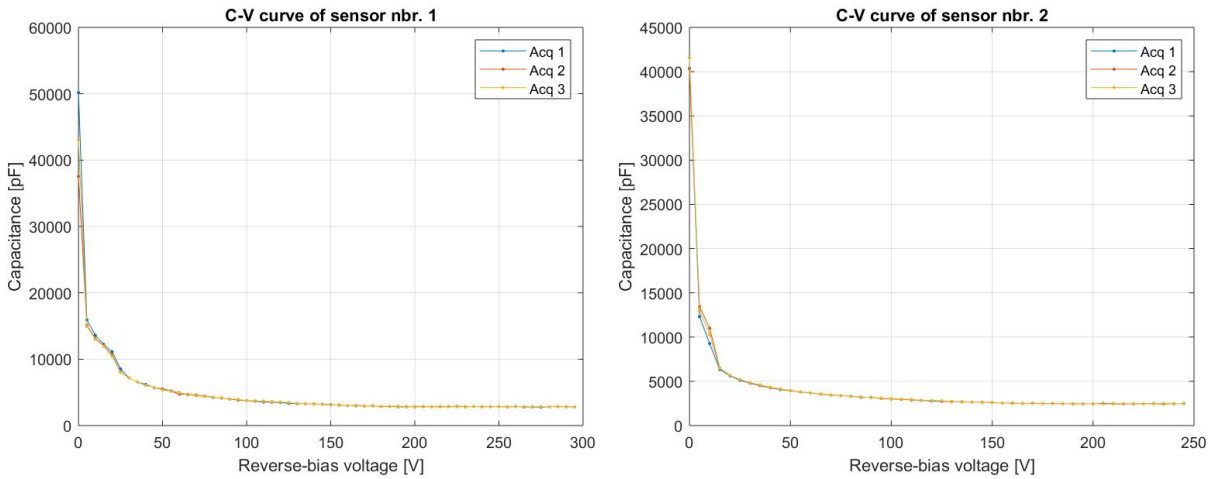


Figure 9.2 – **View focusing on the sensor electrical connections.** The needles connecting the SCB to the sensor are circled in green and the two environmental sensors are circled in blue.

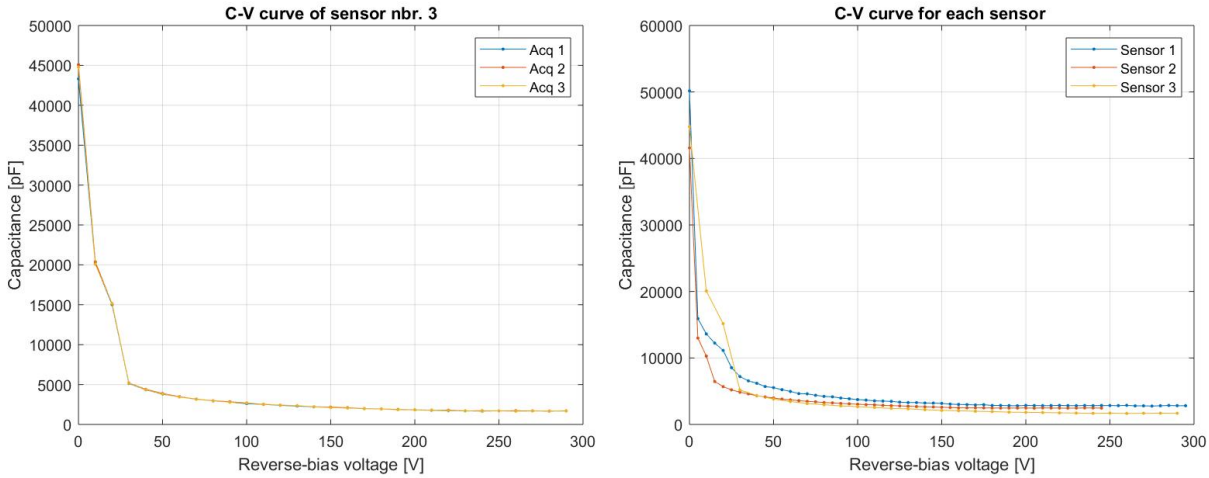
9.1.2 Measurement results

Three *phase-0* sensors have been measured to validate the system. **Sensors 1 and 2 are *modules* connected via their service hybrid and ASIC GND whereas sensor 3 is a *bare* sensor connected via the bias ring and the back-plane**. Three C-V and I-V curves have been measured for each sensor. The measurements have been conducted at room temperature. It should be also noted that the three sensors have different geometries leading to different C-V and I-V curves.



(a) **C-V curves for sensor nbr. 1** (b) **C-V curves for sensor nbr. 2**

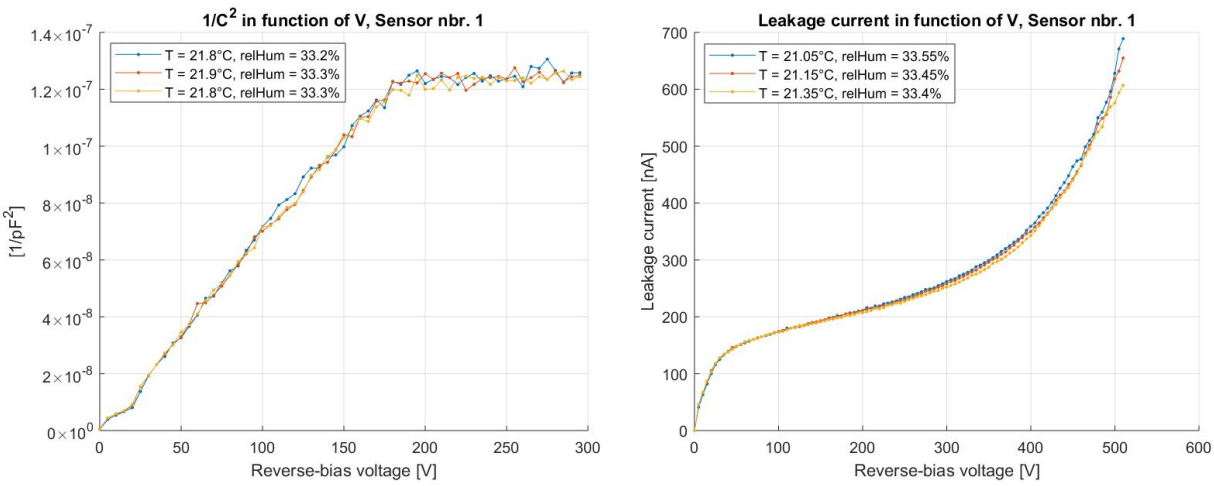
Figure 9.3



(a) **C-V curves for sensor nbr. 3** (b) **C-V curves for all sensors**

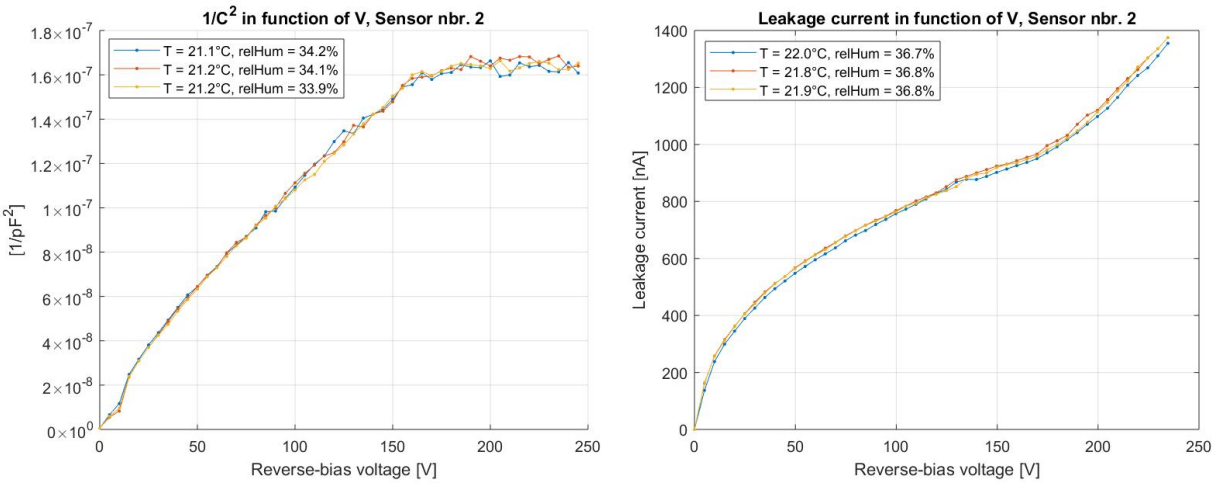
Figure 9.4

For comparison purposes, the C-V curves for each sensor are shown simultaneously in figure 9.4b (one measurement per sensor). Showing the C-V curves as $\frac{1}{C^2}$ in function of V allows the identification of the full-depletion voltage using the method described in section 8.2. The temperature and relative humidity of the environment before starting the acquisition are also reported.



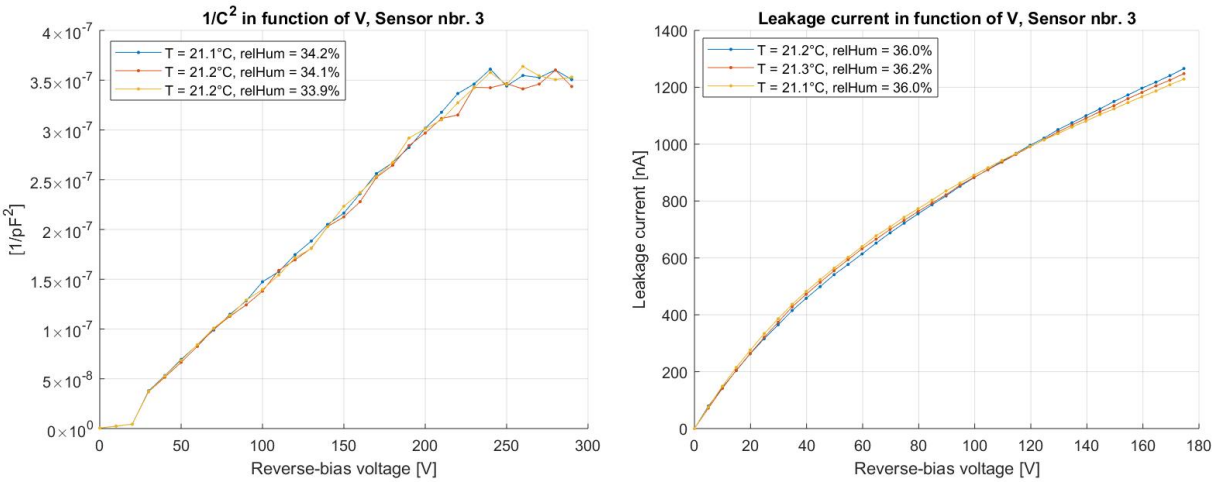
(a) **Full-depletion voltage: 177.8 V** (b) I-V curves of sensor nrb. 1

Figure 9.5 – C-V and I-V curves of phase-0 **sensor nbr. 1**



(a) **Full-depletion voltage: 155.3 V** (b) I-V curves of sensor nrb. 1

Figure 9.6 – C-V and I-V curves of phase-0 **sensor nbr. 2**



(a) **Full-depletion voltage: 234.5 V** (b) I-V curves of sensor nrb. 3

Figure 9.7 – C-V and I-V curves of phase-0 **sensor nbr. 3**

9.1.3 Results discussion

In each case, I-V and C-V curves have been successfully acquired, which validates the system design. The exact specifications of each sensor was not available during the measurements hence *quantitative* comparison cannot be done. A *qualitative* analysis is thus proposed. Sensor 1 has a smaller active volume than sensor 2 (smaller physical dimensions) which in turn has a smaller active volume than sensor 3. Sensor 1 will thus have a larger capacitance at full depletion compared to sensor 2 (the same can be said for sensor 2 with regard to sensor 3). This effect can be seen in figure 9.4b. The I-V curves also reflect this difference in sensor dimension: sensor 1 exhibits less leakage current than sensor 2 which in turn exhibits less leakage current than sensor 3 (see figure 9.8). Additionally, the breakdown of the sensors 1 and 2 can be seen in figures 9.5b and 9.6b.

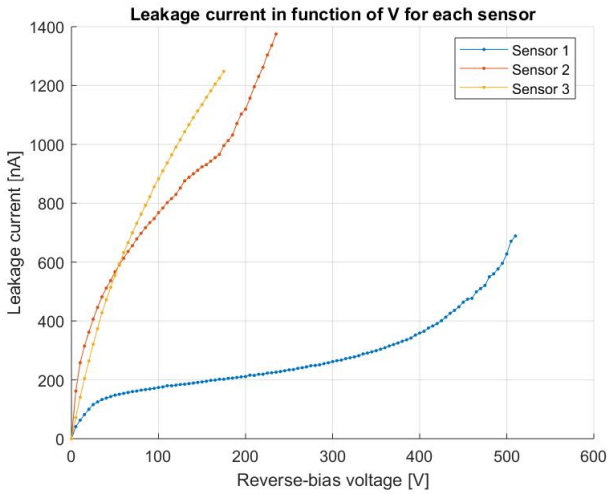


Figure 9.8 – **I-V curve for all sensors**

In the C-V curves of figure 9.4b, an interesting effect occurs at low reverse-bias voltage values: the curves do not follow the $\sim \frac{1}{\sqrt{V}}$ behaviour. This effect is due to the *strip* nature of the sensors and can be explained as follows: at low reverse-bias voltages, the electric field magnitude cannot be considered one-dimensional along the sensor (constant magnitude along the x-dimension in figure 3.6) such that the planar capacitance model of equation 3.5 does not fully hold at low reverse-bias voltages (the interested reader will find a justification of this hypothesis in **appendix E**). But this effect is not present at higher reverse-bias voltages, where the capacitance plateau occurs. Thus, the estimation of the full-depletion voltage is not affected by this effect.

For each sensor, the full-depletion voltage was found using the algorithm described in section 8.2 (see table 9.1). **The full-depletion voltages are within specifications** (must be between 100 and 250V) [23].

Sensor 1	Sensor 2	Sensor 3
177.8V	155.3V	234.5V

Table 9.1 – Full-depletion voltages measured for each sensor

9.2 Testing the SCB at −35°C

For the CMS tracker, the sensors must be characterized at low-temperature (cycles from ambient to −35°C). In most sensor characterization set-ups, the testing instruments are placed outside the industrial fridge (figure 4.1) used to reach the low temperatures and hooked-up to the sensors via wire-passing holes because of two main reasons:

- When submitting printed circuit boards to wide temperature cycles, the solder joints holding each component in place could break, shortening the lifetime of the instrument (e.g. this is a common effect in valve amplifiers as vacuum tubes dissipate a lot of heat, the solder joints of the tube sockets are notorious to crack).

- Even if the selected components used in the instrument are all able to work at low-temperatures, mismatch in amplifiers and comparators could occur which could in turn degrade the measurement performances [24].

Clearly, additional complexity when it is not necessary should be avoided: the instrument built during this project should be placed outside the fridge and should be connected to the sensor under test (inside the fridge) by using the wire-passing holes designed for that purpose. Doing so eliminates risks and expands the lifetime of the SCB.

But one could also want to place the SCB inside the fridge during the tests (e.g. to pass less wires through the wholes in the fridge and to use shorter wires to reduce noise and wire capacitance). To cover this scenario, the board has been tested at $-35°$C inside the fridge. **All the circuits were working correctly** apart from the current measurement circuit because of one op-amp chip (LM358A). Those chips were used as they were already available at the IIHE. Unfortunately, it was found later on that the "A" version of the chip is rated from 0° to 70° C.

This problem can be easily solved by replacing the component with the "B" version (LM358B) which is pin-to-pin compatible and rated from $-40°$ to 85° C. Still, all the other blocks worked: the ADC sampled correctly, the phase-shift measurement circuit was also working, the high-voltage generator was functioning, temperature and humidity sensors were all working and communication with the board was working as before. Additional testings at low-temperatures were not conducted because of limited time.

9.3 Total measurement time

As explained in the introduction, the IIHE is expected to produce more than 2500 sensor modules, each module embedding two Silicon strip sensors connected in parallel and measured simultaneously (a total of $N_{meas} \sim 2500$ measurements). In the future, an experimental set-up, built around the system developed during this thesis will be deployed to characterize all 5000 Silicon strip sensors.

It is of interest to estimate the time that the complete measurement campaign will take. The time to acquire the I-V and C-V curve $T_{iv,cv}$ of **one sensor** is approximately $T_{iv,cv} = 20$ minutes with a voltage step of 1V (finest voltage step that the system offers). The sensors must preferably be measured at $-35°$C: the industrial fridge (figure 4.1) takes approximately 2 hours to reach $-35°$C and a similar time to reach room temperature again ($T_{fridge} \sim 4$ hours in total). **This is a considerable bottleneck** as the sensors to characterize must be placed inside the fridge at room temperature, characterized at $-35°$C and then be removed at room temperature (one cannot open the fridge at $-35°$C because condensation will damage the sensors).

The measurement process can be accelerated by measuring N_{batch} sensors in the same temperature cycle. Considering $N_{batch} = 5$ sensors measured at the same time, the total measurement time T_{total} can be estimated using equation 9.1 (table 9.2 summarizes the parameter values).

N_{meas}	N_{batch}	$T_{iv,cv}$	T_{fridge}
2500	5	20 min	4 h

Table 9.2 – Measurement campaign parameters.

$$T_{total} = \frac{N_{meas}}{N_{batch}}(T_{iv,cv} + T_{fridge}) \tag{9.1}$$

Dividing T_{total} by the typical number of hours in a workday ($\sim$ 8 hours), **it will take 271 days to finish characterization for all the 2500 sensor modules**. As said earlier, the time taken by the fridge is the bottleneck such that the measurement time taken by the measurement instrument can be ignored (4 hours v.s. 20 minutes). **Therefore, one should maximize the number of sensors measured in parallel (N_{batch}) or relax the temperature constraints**.

9.4 Conclusion

In this chapter, I-V and C-V curves acquired using the complete system designed during the thesis were shown. **The main goal of this thesis was thus successfully achieved.** The acquired C-V ad I-V curves were also compared and discussed. **This chapter experimentally validated the complete design of the system.**

Chapter 10
Conclusion

The high-luminosity phase of the LHC is expected to be operating in 2026. In order to comply with the highly radioactive environment imposed by HL-LHC, the CMS detector needs an upgrade. CMS is composed of a plethora of sub-detectors and this thesis focused on the *phase-2 upgrade* of the particle-tracking Silicon sensors.

Indeed, the IIHE department of the ULB/VUB is expected to produce more than 2500 Silicon tracker modules. Thus, the design and implementation of a custom sensor characterization setup is highly desired. Having such system is crucial for the validation of each sensor to be deployed at CERN.

The design, implementation and experimental validation of such setup under tight time and specification constraints was a considerable challenge, although **successfully tackled during the project**.

First, the thesis introduced the engineering problem to be tackled and the target specifications. Then, the LHC update project and its link with the master thesis was detailed. After that, the working principle of Silicon sensors was introduced to set the theoretical background needed for the design of the instrument (SCB) and for the various sensor models used throughout the design. The link between the full depletion voltage and the plateaus in I-V/C-V curves of sensors was also made. Then, a bird's eye view of the complete system composed of the SCB, the interface software and the industrial fridge was shown, before focusing on the design of each building block (high-voltage generator, current measurement circuit and capacitance measurement circuit). Finally, signal processing cues used within the interface software were discussed and the complete system was validated using three *phase-0* Silicon strip sensors.

The experimental validation demonstrated that **the system was capable of acquiring the I-V and C-V curves** with more than enough precision (leakage current resolution: ~ 4 nA, relative error on capacitance measurement: < 0.32 %, measurement time < 20 minutes). Furthermore, low temperature ($-35°$C) testing showed that all the building blocks of the board were working correctly apart from one component which was not rated for temperatures below 0°C (an issue easily solved by replacing the component by its "B" version).

As **future perspective**, the system needs to be replicated in order to measure multiple sensors at the same time, the interface software should be integrated in the existing CMS software suite for sensor characterization (so-called *phase-2 ACF*). A third revision of the board is also needed to embed the sine wave generator in the instrument itself. For that purpose, the firmware should be extended to support sine wave generation. Finally, a measurement campaign should be planned and conducted for the 2500 sensor modules.

During this master thesis project, the bulk of the work was finished ahead of time and allowed the author to present his work during inter-university CMS meetings **and at an international workshop on Silicon sensors in Vienna** (TREDI 2020 "Trento" Workshop, see appendix H), on behalf of the whole team. The work even made some impact in the community as the particle physics group of **ETH Zurich took contact with the author** to gather more details about the design, in order to build their own testing set-ups.

In conclusion, the system designed during this project will be extended and integrated into a large-scale testing set-up which will enable the characterization of more than 2500 sensor modules for their deployment at CERN.

Appendix A

Discussion on the effect of windowing for spectral analysis

In order to proceed to a spectral analysis with an instrument such as an oscilloscope or a spectrum analyser, the incoming signal has to be sampled and projected into the Fourier basis using a discrete Fourier transform (DFT) which consists on the following transformation.

First, the continuous-time signal $x(t)$ is sampled at a certain sampling period T_s which results into the following discrete-time signal.

$$x_d[n] = x(nT_s) \tag{A.1}$$

Where n is an integer and x_d is the discrete-time signal obtained by sampling $x(t)$. In continuous-time, the Fourier transform is defined as follows.

$$X(f) = \int_{-\infty}^{+\infty} x(t)e^{-j2\pi ft}dt \tag{A.2}$$

In order to obtain the discrete Fourier transform, the integral becomes a sum and the time t gets sampled. The general definition of a N point DFT is the following.

$$X_d[k] = \sum_{n=0}^{N-1} x_d[n]e^{-j2\pi\frac{kn}{N}} \tag{A.3}$$

Where $X_d[k]$ is the N-point result of the DFT, N is the number of samples of $x_d(n)$ and k is the discrete frequency (between 0 and $N-1$).

Of course, $x_d(n)$ has to contain an infinite number of samples to correctly represent the continuous-time signal $x(t)$ but it is not practical to work with infinite sequences, that is why the sequence is truncated to N points. Truncating the sequence is equivalent to multiplying the original sequence with a so-called *rectangular window*.

Thus, the N-point DFT derived above assumed the use of a rectangular window w_{rect}.

$$w_{rect} = \begin{cases} 1 & 0 \leq n \leq N-1 \\ 0 & \text{elsewhere} \end{cases} \tag{A.4}$$

The truncated sequence is thus given by the following equation.

$$x_d[n] = x[n]w_{rect}[n] \tag{A.5}$$

Which, in the frequency domain, results in the convolution of the desired spectrum with the spectrum of the window.

$$X_d(\omega) = X(\omega) * sinc(\frac{\omega T}{2}) \tag{A.6}$$

Thus, the use of a regular rectangular window distorts the desired spectrum. This phenomenon is called *leakage*. As a *sinc* function is placed at the location of every impulse of the original spectrum (which is the action of convolution), each excited frequency leaks some of its energy to other frequencies.

One of the important effect of the leakage apart from the fact the spectrum is distorted is the lowering of spectral amplitude at the excited frequencies due to Parseval's theorem (which states that the power of the signal after a DFT operation is conserved).

To counteract the effects of leakage, it is possible to use other types of window like the *Blackman window* used within this project [19]. The frequency spectrum of those bell-shaped windows are such that their side lobes in the frequency domain decrease significantly faster than the side lobes of the *sinc* function as shown in figure A.1.

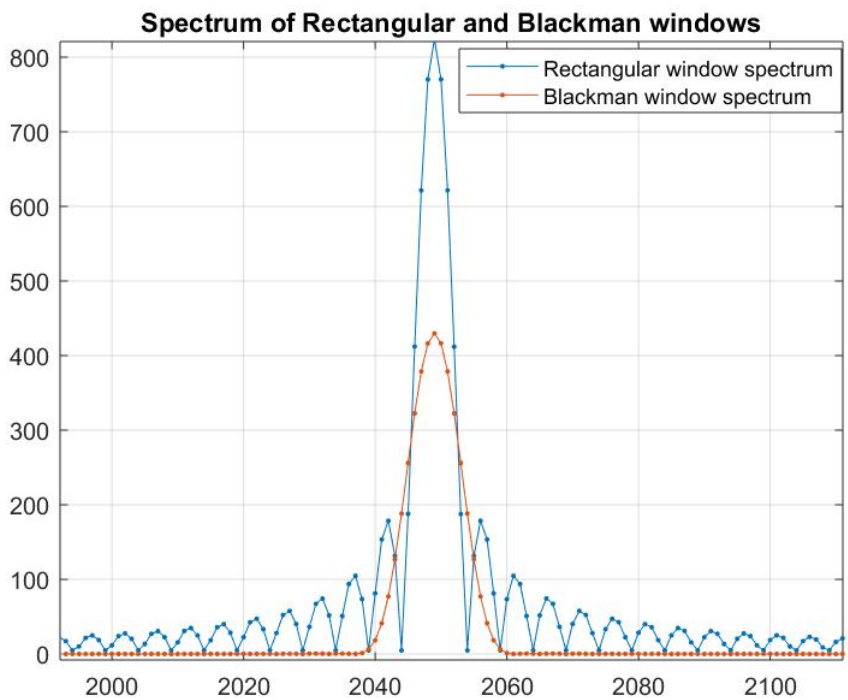


Figure A.1 – **Spectrum of the Rectangular and Blackman windows.** The Rectangular window has significantly more side lobes in the frequency domain compared to the Blackman window.

This results in a reduced amount of leakage from one frequency bin to the others.

It is still important to note that, while bell-shaped windows reduce leakage, their main lobe is wider than the main lobe of the *sinc* function which lowers the frequency resolution

of the final spectrum. Furthermore, the use of a bell-shaped window attenuate the total energy of the signal to analyse. This attenuation is compensated by dividing the window by its RMS value prior to its application to a signal.

Appendix B

Discussion on the processing gain provided by the DFT

In this project, spectral analysis has been used to provide an increase in SNR for the excitation current measurement. This gain stems from the fact that the DFT of white noise (and *stationary* coloured noise) is *uncorrelated* over the frequency bins. This is proven below by defining v_n as the noise sequence in the time domain [25].

The DFT of v_n is defined as follows:

$$V_k = \sum_{n=0}^{N-1} v_n e^{-j2\pi \frac{kn}{N}} \tag{B.1}$$

As v_n is stochastic, the expected value of B.1 must be considered:

$$E\{V_k\} = \sum_{n=0}^{N-1} E\{v_n\} e^{-j2\pi \frac{kn}{N}} \tag{B.2}$$

The covariance matrix of V_k is then defined as follows:

$$E\{V_k V_l^*\} = E\{\Re(V_k)\Re(V_l)\} + E\{\Im(V_k)\Im(V_l)\} + E\{\Im(V_k)\Re(V_l)\} - E\{\Re(V_k)\Im(V_l)\} \tag{B.3}$$

Each term of B.3 lead to equations B.4, B.5 and B.6 where δ_{kl} denotes the *Kronecker delta*.

$$E\{\Re(V_k)\Re(V_l)\} = \frac{N}{2}\sigma_v^2 \delta_{kl} \tag{B.4}$$

$$E\{\Im(V_k)\Im(V_l)\} = \frac{N}{2}\sigma_v^2 \delta_{kl} \tag{B.5}$$

$$E\{\Im(V_k)\Re(V_l)\} = E\{\Re(V_k)\Im(V_l)\} = 0 \tag{B.6}$$

Equations B.4 and B.5 show that the noise is uncorrelated over the frequency bins. One can thus safely perform analysis *frequency-bin per frequency-bin* without loss of information. Additionally, equations B.4 and B.5 show that the *standard deviation* of the noise increase as $\sim \sqrt{N}$ after an N-point DFT.

On the other hand, it can be proven [25] that the DFT of a periodic signal grows $\sim N$ such that the gain in SNR (compared to the SNR of a measurement in the time domain SNR_1) scales following equation B.7.

$$SNR_N = \frac{N^2 \sigma_{sig}^2}{N \sigma_v^2} = N \times SNR_1 \tag{B.7}$$

This processing gain can be intuitively understood as follows: by increasing the number of measurement samples N, the periodic signal remains unchanged after a DFT as it keeps occupying its frequency bins. On the other hand, noise is *redistributed* over the available bins in a way such that its *total energy remain unchanged*. In each frequency bin, the noise amplitude become smaller by increasing N which leads to an increase of SNR when measuring the periodic signal from its frequency bins [25].

Appendix C

Quantization noise in uniform quantizers

A uniform quantizer is defined as a quantizer exhibiting the same quantization step δq along the whole quantization range [17]. Being a non-linear operation, quantization introduces an error on a sampled signal s. This error can be modelled as an *additive noise term with uniform distribution* z_q (equation C.1).

$$s_q = s + z_q \tag{C.1}$$

Figure C.1 shows the probability density function $f(x)$ of the quantization noise z_q.

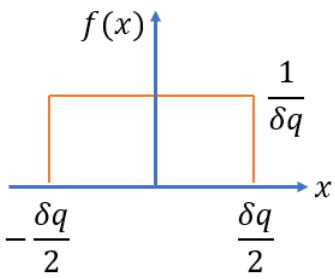


Figure C.1 – Probability density function of uniform quantization noise.

The noise variance σ^2 is derived in equation .

$$\sigma^2 = \int_{-\frac{\delta q}{2}}^{\frac{\delta q}{2}} x^2 \frac{1}{\delta q} dx = \frac{\delta q^2}{12} \tag{C.2}$$

The relation of equation C.2 can be used to estimate the effective resolution δq of a quantizer from the variance σ^2 of the quantization error.

Appendix D

Least-squares Linear Regression

The least-squares linear estimator is defined as a function $f(x_0, x_1, ..., x_N) : \mathbb{R}^N \mapsto \mathbb{R}$ linear in the parameters such that:

$$y = f(\underline{x}) = \underline{X}\ \underline{\theta}^t \tag{D.1}$$

With:

$$\underline{X} = \begin{bmatrix} \underline{x}^t & 1 \end{bmatrix} \tag{D.2}$$

and $\underline{\theta}$ are the parameters of the linear model and t denotes the transpose operation. Given a set of M labelled data $(y_i, \underline{x}_i)$, two matrices Y and X can be formed as follows:

$$Y = \begin{bmatrix} y_0 \\ y_1 \\ . \\ . \\ . \\ y_M \end{bmatrix} \tag{D.3}$$

$$X = \begin{bmatrix} \underline{x}_0^t & 1 \\ \underline{x}_1^t & 1 \\ . & \\ . & \\ . & \\ \underline{x}_M^t & 1 \end{bmatrix} \tag{D.4}$$

The linear regression aims to approximate the relation between Y and X as follows (where ϵ denotes the error):

$$Y = X\underline{\theta}^t + \epsilon \tag{D.5}$$

$$\hat{\theta} = \underset{\theta}{\operatorname{argmin}} ||Y - X\underline{\theta}^t||_2^2 = (Y - X\underline{\theta}^t)^t (Y - X\underline{\theta}^t) \tag{D.6}$$

The optimisation problem of equation D.6 is solved by forcing the derivative of the error $||\epsilon||_2^2$ with respect to θ to zero.

$$\frac{\partial ||\epsilon||_2^2}{\partial \theta} = -2X^tY + 2X^tX\theta \tag{D.7}$$

$$\theta = (X^tX)^{-1}X^tY \tag{D.8}$$

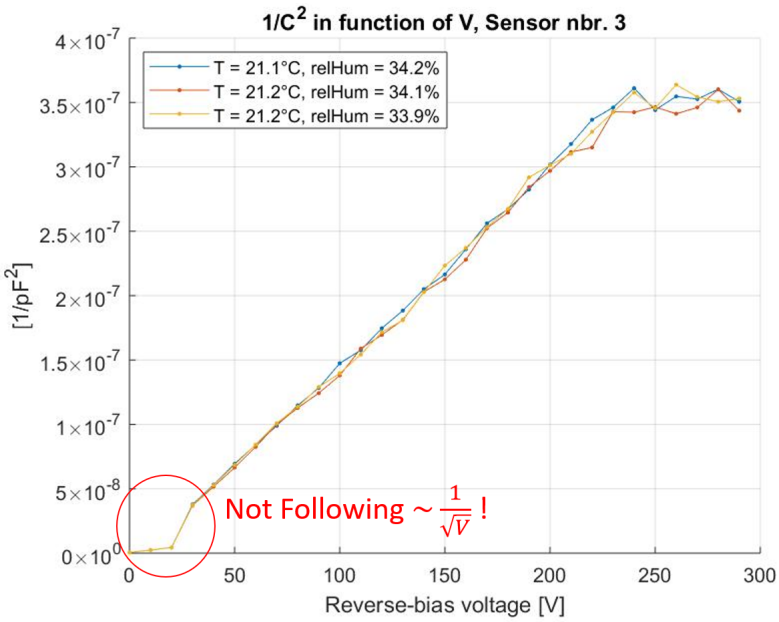
For sake of completeness, it should be pointed out that equation D.8 is non-singular if $M > N$ that is, if the number of training data is higher than the number of parameters to estimate. The use of this simple regression rule was enough for this project as the relation

between $\frac{1}{C^2}$ and reverse-bias voltage V was known to be linear upfront. If this is not the case, a higher-order model should be selected and regularisation on the model coefficients should be introduced (by the mean of *Ridge* or *LASSO* regression) [22].

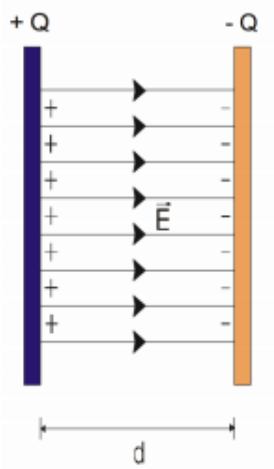
Appendix E

Electric field distribution along the sensors at low reverse-bias voltage

An interesting effect was seen on the C-V curve acquired using the *phase-0* Silicon strip sensors: the curves were not following a $\sim \frac{1}{\sqrt{V}}$ behaviour at low reverse-bias voltages. For instance, this effect can be seen for sensor number 3 in figure E.1a. In this appendix, a hypothesis for this deviation is proposed.



(a) $\frac{1}{C^2}$ in function of V for sensor 3.



(b) Parallel plate model

[26]

Figure E.1

In this project, the measurements are physically interpreted using the parallel plate model (figure E.1b) leading to equation E.1 [26].

$$C = \frac{\epsilon A}{d} \tag{E.1}$$

In chapter 3, the $C \sim \frac{1}{\sqrt{V}}$ relation was derived for the equivalent capacitance of a P-N junction under reverse-bias voltage V, assuming the parallel plate model. So, the $C \sim \frac{1}{\sqrt{V}}$ behaviour for the Silicon strip sensors corresponds to **the hypothesis** that the parallel plate model can be applied which is **not the case** at low reverse-bias voltages. Figure E.2 and E.3 show qualitative examples of the electric field distribution inside the depletion zone of strip sensors **at low and high reverse-bias voltage**.

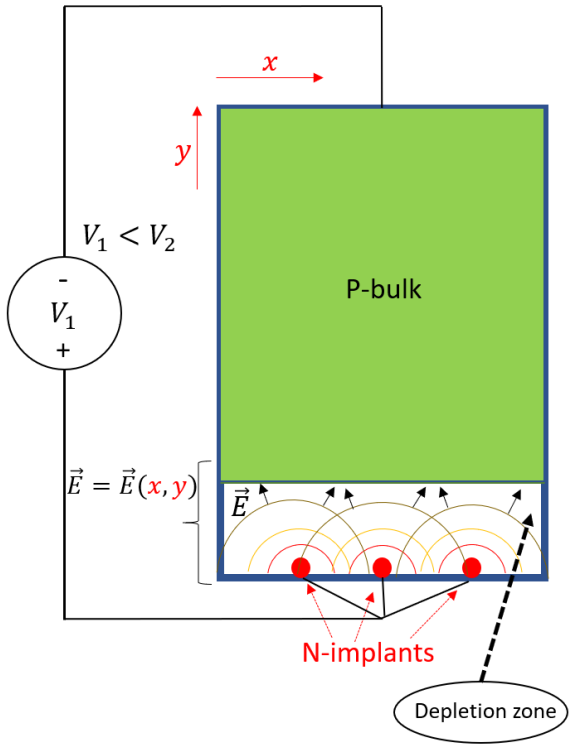


Figure E.2 – Electric field distribution inside a strip sensor with a **low reverse-bias voltage**.

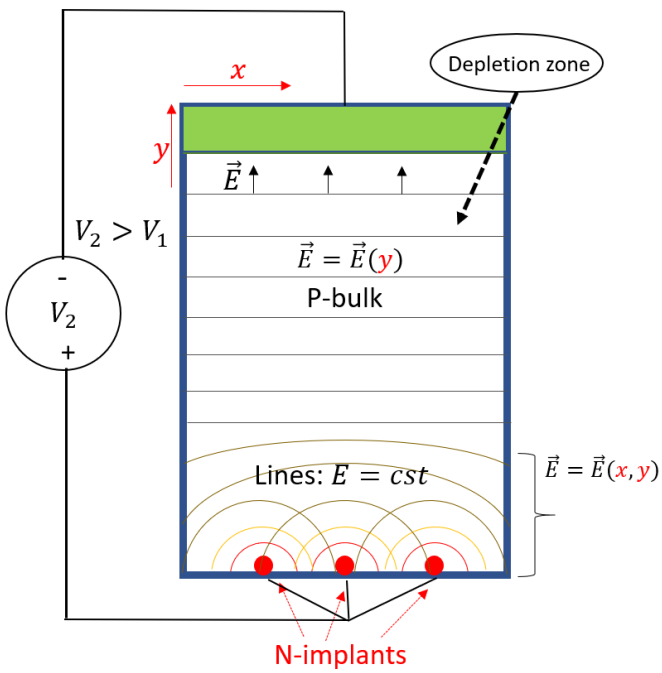


Figure E.3 – Electric field distribution inside a strip sensor with a **large reverse-bias voltage**.

In figures E.2 and E.3, the terminals of the equivalent capacitor are formed by the

strips (N-implants) and the lower surface of the P-bulk. By applying a reverse-bias voltage, implants become negatively charged and the P-bulk side becomes positively charged in a uniform manner. At each implant, the charge can be considered as a **point charge** Q. The electric field $\vec{E}$ at the implant side is thus radial and follows equation E.2.

$$\vec{E} \sim \frac{Q}{r^2}\vec{1_r} \tag{E.2}$$

When applying a **small reverse-bias voltage** (figure E.2), the depleted zone is small such that the two terminals of the equivalent capacitor are close to each other. Figure E.2 shows that the distribution of $\vec{E}$ is **bi-dimensional** ($\vec{E} = \vec{E}(x, y)$) and so, **not planar**. ***The parallel plate model for the capacitance cannot be applied.***

On the other hand, the depleted zone is large at high reverse-bias voltage such that the two terminals of the equivalent capacitor are far from each other. Figure E.3 shows that the distribution of $\vec{E}$ is **bi-dimensional** (i.e. $\vec{E} = \vec{E}(x, y)$) near the implant side but quickly becomes **one-dimensional** (i.e. planar, $\vec{E} = \vec{E}(y)$) **for the largest part of the depleted zone** (as the radius r becomes very large). In the planar part of sensor where $\vec{E} = \vec{E}(y)$, the parallel plate model for the capacitance **can be applied** while this model **cannot be applied** for the bi-dimensional part where $\vec{E} = \vec{E}(x, y)$ as usual.

For the case of figure E.3 (high reverse-bias voltage), the equivalent capacitor of the sensor can be divided into two capacitors in series C_0 and C_1 where C_0 models the capacitance of the region where the parallel plate model **cannot be applied** and C_1 models the capacitance of the region where the parallel plate model **can be applied** (see figure E.4).

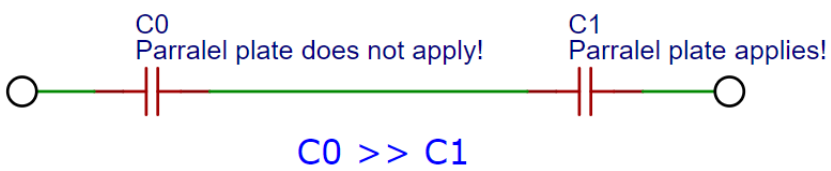


Figure E.4 – Modelling the equivalent capacitor of the sensor under **high reverse-bias voltage**.

The region corresponding to C_0 is very small compared to the region corresponding to C_1. C_0 is thus significantly larger than C_1 such that equation E.3 holds for the circuit of figure E.4.

$$C_{series} = (\frac{1}{C_0} + \frac{1}{C_1})^{-1} \approx C_1 \tag{E.3}$$

Thus, the capacitance of the sensor under high reverse-bias voltage is dominated by C_1 **where the parallel plate model applies**.

In conclusion, the qualitative analysis discussed above showed that at low values of reverse-bias voltage, the parallel plate model for the capacitance cannot be applies as the field configuration is not one-dimensional. On the other hand, the analysis showed that the parallel plate model can be applied for large reverse-bias voltages. This explains why the C-V curve of the *phase-0* Silicon strip sensors measured during the project were not following the $\sim \frac{1}{\sqrt{V}}$ behaviour for small values of reverse-bias voltage.

Appendix F

ARM Cortex-M3 based PSOC micro-controller

In this project, a CY8C5888LTI *Programmable System-on-Chip* (PSOC) from Cypress has been used as the central micro-controller. This PSOC features configurable analog and digital peripherals as well as a 32-bit ARM Cortex-M3 core which make this chip well suited for embedded data acquisition tasks.

This appendix will first give an overview of the PSOC chip and its building blocks before going into the details of the ARM Cortex M3 architecture.

F.1 The CY8C58LP family of Cypress PSOC

The PSOC chip used within this project provides configurable analog, digital and interconnect circuitry, built around an ARM Cortex-M3 CPU. Figure F.1 shows the block diagram of the chip.

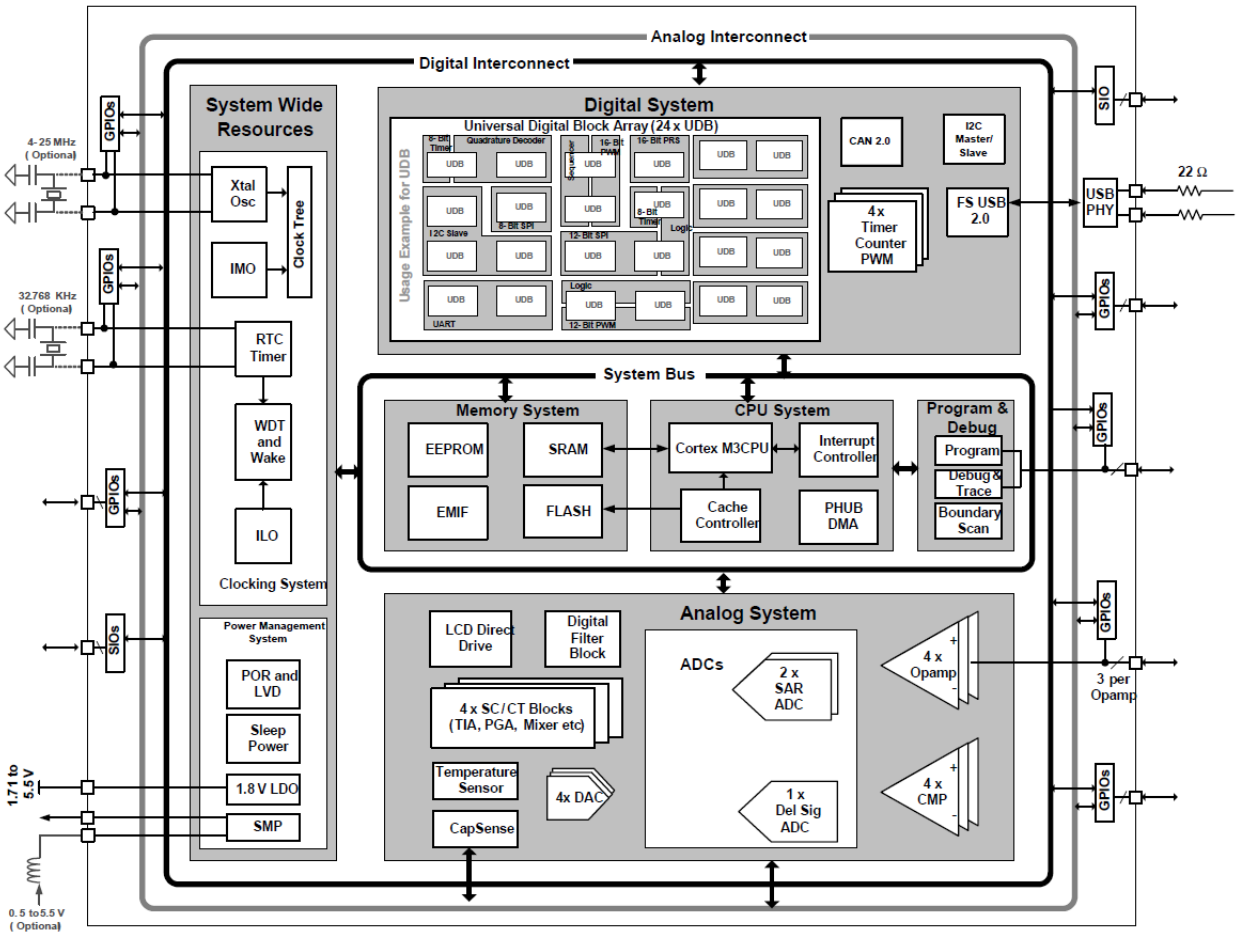


Figure F.1 – Block diagram of the PSOC chip used within this project [6].

Starting from top-left, the *System Wide Resources* block handles the **clock generation and distribution** to the processing block composed of the *memory system*, *CPU system* and *Program/Debug* block. Two clocks are available: the main system clock (up-to 80 MHz) and a *low-frequency* clock used for watchdog timer (resets the processor if instruction execution is stuck), sleep timer and ultra low-power system clock for the CPU ($P \sim C_{in}F_{clk}V^2$). The main system clock can use the *Internal Main Clock* (IMO) or an external oscillator. The system frequency can be adjusted using the integrated PLL. The low-frequency clock can be generated via the *Internal Low-frequency* Oscillator (ILO) or by the means of an external oscillator. The *Power Management System* block (bottom-left) generates the voltage rails needed for all the blocks in the chip. The chip supports a voltage supply range of 1.71 to 5.5 V.

Moving to bottom-right in figure F.1, the *Analog System* block provides *configurable* analog and mixed-signal circuitry which can be routed in a user-defined manner to any GPIO pin of the chip. The *Analog System* features blocks such as delta-sigma and SAR ADCs, 8-bit DACs, comparators, opamps, mixers and modulators. Figure F.3 shows the Analog subsystem block diagram.

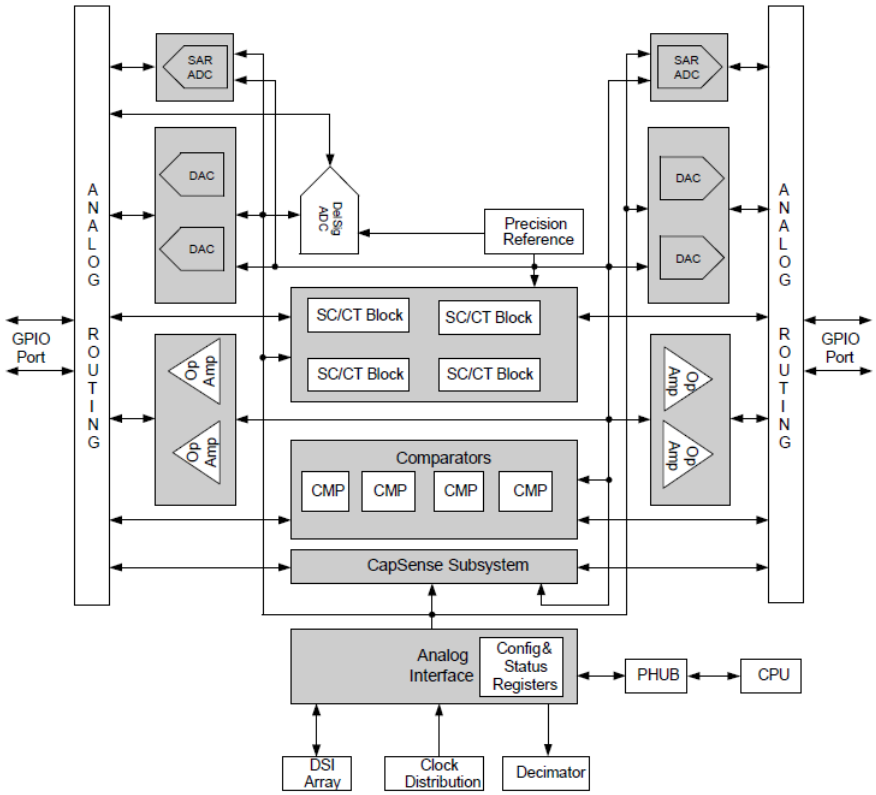


Figure F.2 – Analog subsystem block diagram [6].

The *Digital System* block (top-right) connects any peripheral (SPI, I2C, UART and so on) to any GPIO pin. It also provides 24 User Defined Blocks (UDB). Each UDB contains

two programmable logic arrays (figure F.3) which can be used to form state machines or to provide combinational logic. The *Digital System* can be used to deploy timers, counters, PWM blocks and so on. Figure F.4 shows the UDB block diagram.

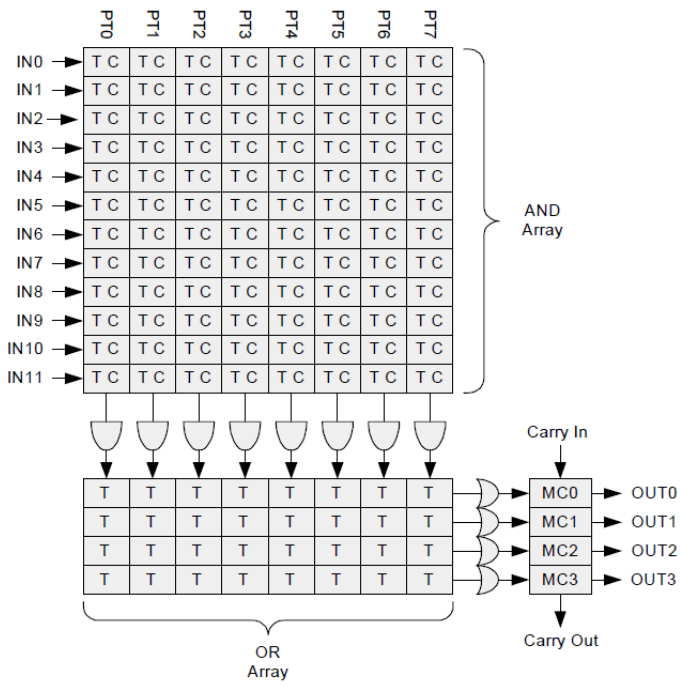


Figure F.3 – Programmable Logic Array architecture. 12 inputs can be arbitrary AND-ed together giving eight product terms. Each product term can then be arbitrary OR-ed together giving four sum terms [6].

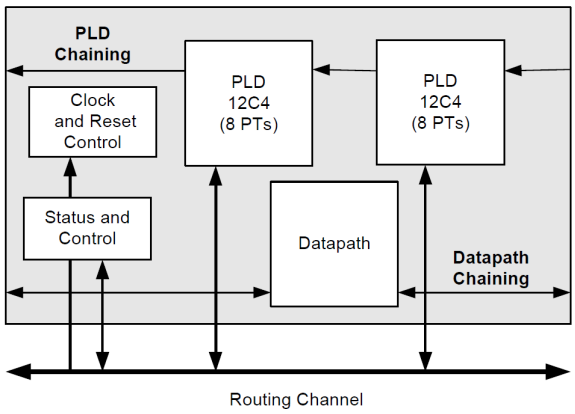


Figure F.4 – UDB block diagram. The *Datapath* block contains structured logic to implement compare-type configurations and condition generation. The *Status and Control* module allows the CPU to interact with the UDB [6].

Both the *Analog System* and the *Digital System* are **controlled by the processing block** (*memory system*, *CPU system* and *Program/Debug* blocks in figure F.1). The processor is built around an ARM Cortex-M3 CPU and will be detailed in the next section.

F.2 ARM Cortex-M3 Core

The **memory sub-system** of the processing block is composed of the *program flash memory* (256 kByte), an additional *flash memory for error correcting codes* (32 kByte), 64 kByte of *RAM* and an additional *EEPROM* (2 kByte) to store variables generated by the program execution between power cycles (as the *RAM* is erased when the chip is not powered anymore).

The **debugging/programming sub-system** supports *JTAG* (5-pin protocol, supports device chaining) and *SWD* (2-pin protocol, does not support chaining). The debugging interface supports six program address breakpoints and two literal (i.e. a memory location related to the current *program counter* value during execution) access breakpoints. The **ARM Cortex-M3** is 32-bit (which defines data/instruction bus widths, register sizes and ALU width), three-stage pipelined (*fetch*, *decode* and *execute*) based on a *Harvard architecture* (instruction and data memory separated in *RAM* and accessed by two distinct buses which enhances memory-CPU bandwidth). The CPU delivers an average MIPS in function of clock frequency of 1.25 DMIPS/MHz and implements the *Thumb-2 Instruction Set Architecture* (ISA) [27].

Figure F.5 shows the block diagram of the *CPU*.

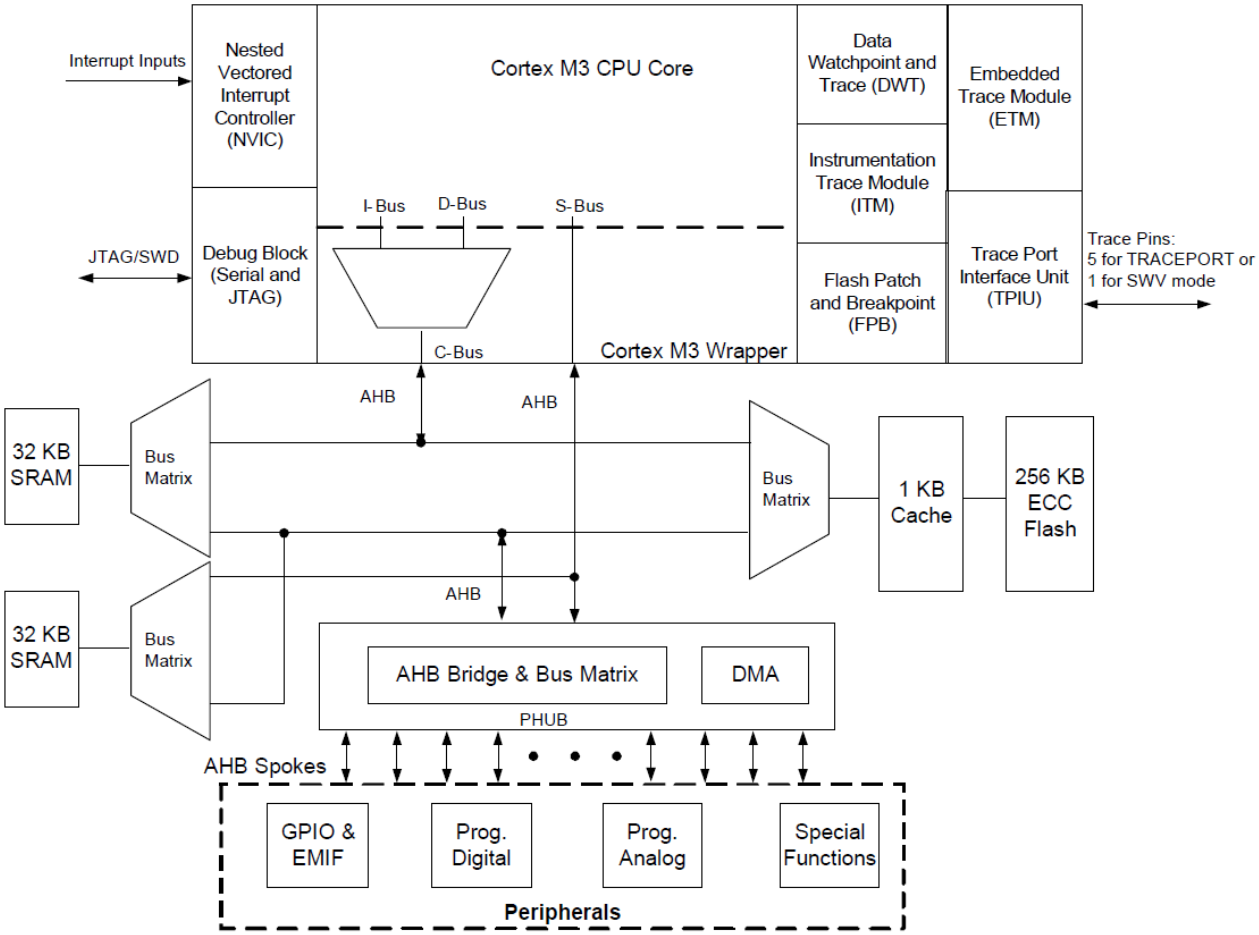


Figure F.5 – CPU block diagram [6].

Starting from top-right in figure F.5, the *tracing* modules (used for logging of data about program execution, data watchpoint to monitor events during debug and so on) are tightly interconnected with the CPU.

The program flash memory (middle-right) is interfaced by the CPU through a 1 kByte *cache memory* to improve instruction execution rate and reduce system power consumption as less flash accesses are required. In addition, the cache is 4-*way set-associative* to further reduce cache miss rate.

The bottom part of figure F.5 shows the interconnection of the CPU with the peripherals via the so-called *Advanced High-performance Bus* (AHB) which connects the peripherals with the CPU system bus (S-Bus), the memory buses and the *Direct Memory Access* (DMA) block via the *PHUB* block.

The PHUB block (hub interconnecting peripherals, memory and CPU together) can be controlled by the *CPU* or by the *DMA* (enabling peripheral communication without CPU intervention). The CPU always has higher priority than the DMA when accessing the same resources and eight different levels of priority can be assigned to each DMA channel.

The middle-left part of figure F.5 shows the interconnection between the CPU and the *RAM*. As the CPU follows a Harvard architecture, the 64 kByte RAM is divided in two 32 kByte chunks for separated data and instruction memories.

Moving to the top-left part, the *debugging/programming* module (JTAG and SWD) and the *interrupt controller* block are shown. The interrupt controller provides *nested interrupt support* (i.e. interrupts can be programmed to different priority levels) as well as *vectored interrupt support* (i.e. the starting address of the interrupt service routine or ISR is read from a vector table in memory such that there is no need to specify the starting address of the ISR in firmware, which in turn makes the interrupt request faster). The so-called *Nested Vectored Interrupt Controller* (NVIC) supports 16 system exceptions (like reset, bus fault and so-on) and 32 peripheral interrupts.

Finally, the *Cortex-M3 core* is shown on the top-side of figure F.5 and contains the registers, the *ALU*, the data path and the bus interfaces.

F.3 Conclusion

The CY8C5888LTI PSOC is well suited for this project as it embeds configurable analog and digital circuitry with an ARM Cortex-M3 core. The configurable analog and digital blocks help reducing the bill of material of the design and the ARM Cortex-M3 core provides higher processing performance compared to traditional 8-bit micro-controllers.

In this project, a PSOC *System On Module* (SOM) (CY8CKIT-059) has been used (see figure F.6).

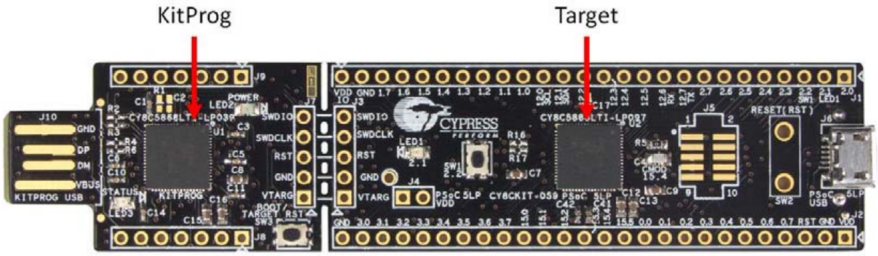


Figure F.6 – CY8CKIT-059 SOM.

The PSOC SOM has been integrated to the PCB via the *MCU socket* (see figure 4.2) as the chip package (QFN) makes it hard to solder manually and as the SOM conveniently embeds the programmer/debugger (KitProg in figure 4.2).

Appendix G

The $\Delta\Sigma$ ADC

In this project, a $\Delta\Sigma$ ADC has been used in the high-voltage generation and regulation circuit. This type of ADC is used when a fine quantization resolution is needed. This appendix details the working principle of the $\Delta\Sigma$ ADC.

Figure G.1 shows the block diagram of the $\Delta\Sigma$ ADC.

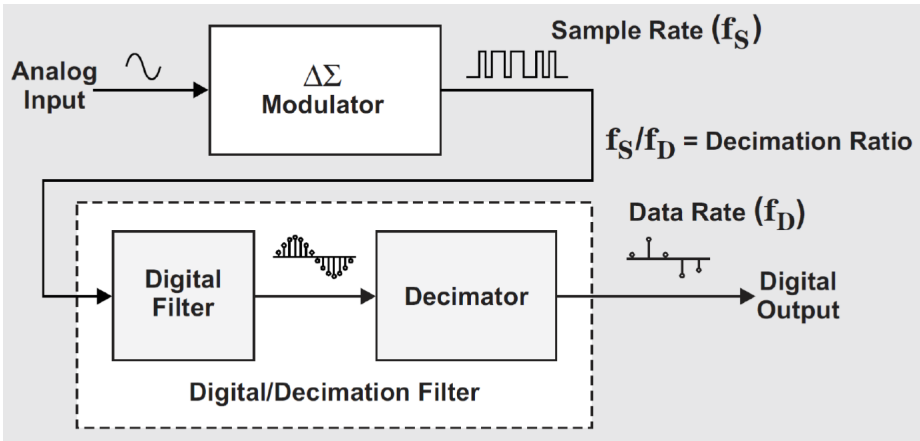


Figure G.1 – Block diagram of the $\Delta\Sigma$ ADC [7].

The input signal to be quantized is first fed to a $\Delta\Sigma$ *modulator* which outputs a binary (digital) signal representing the input signal. The sampling frequency of the $\Delta\Sigma$ modulator f_s is chosen higher than the desired Nyquist sampling rate f_D to provide a high *signal to quantization noise* ratio (which defines the effective bit-count of the ADC) [7].

Then, the binary signal is fed to a *digital filter* (with the same sampling frequency of f_s) which will low-pass filter the binary signal coming from the $\Delta\Sigma$ *modulator* and code its output using a certain number of bits (e.g. 16-bit).

Finally, as the sampling rate f_s is higher than the desired Nyquist rate f_D, the output of the *digital filter* is decimated and the quantized signal is obtained.

The following sections detail the background theory and the building blocks of figure G.1.

G.1 Signal to quantization noise ratio

Considering a sine-wave which spans the complete range of an N-bit ADC, the *signal to quantization noise* (in dB) over the Nyquist bandwidth is given by equation G.1 [17].

$$SNR[dB] = 6.02N + 1.76dB \tag{G.1}$$

Equation G.1 can be used the other way around such that for a given SNR, one can derive the effective number of quantization bit N [7].

A straight-forward way to provide a gain on the SNR is to use a higher sampling rate (but keeping the same Nyquist bandwidth by the use of an anti-aliasing filter), as the same noise power will be distributed over a higher amount of frequency bins such that for a two-time oversampling, the SNR will gain 3dB. Using equation G.1, **an oversampling of four-time** is approximately needed to improve the effective number of bit by 1.

But in practice, one cannot improve the effective number of bit by a large amount using traditional ADCs with oversampling. For instance, if 12-bit resolution is needed starting from a 4-bit ADC at 1GS/s, the oversampling factor should be $4^{(12-4)}$ (as each oversampling by a factor of 4 improves the effective number of bits by 1). **Thus, a sample rate of 65.536 TS/s is needed which completely impractical**.

The $\Delta\Sigma$ ADC overcomes this problem by providing *a higher improvement on the number of effective bits* for the same oversampling ratio.

G.2 The $\Delta\Sigma$ modulator

Figure G.2 shows the topology of a first-order $\Delta\Sigma$ modulator. The order of the modulator is defined as the number of integrator in the forward loop.

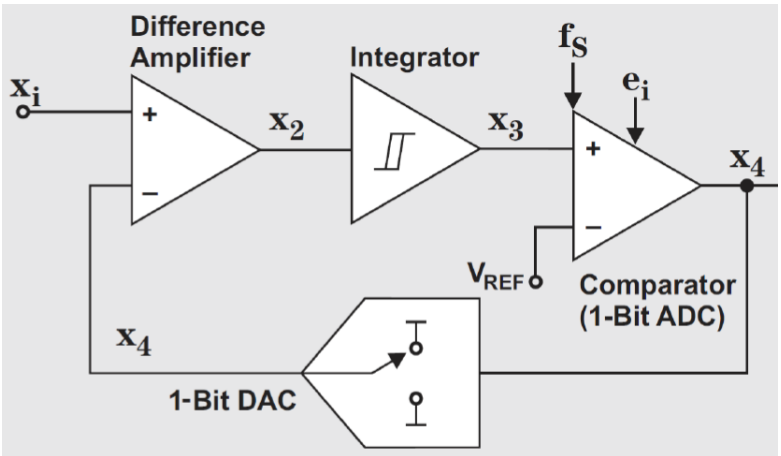


Figure G.2 – First order $\Delta\Sigma$ modulator [7].

The analog signal to be quantized is first fed to the difference amplifier which outputs the error x_2 between the input x_i and output signal x_4. This error signal x_2 is then fed to an integrator with a transfer function given by equation G.2.

$$H(s) = \frac{\omega_p}{s} \tag{G.2}$$

The output of the integrator x_3 is then quantized by a **1-bit ADC** implemented as a synchronous comparator working at the *oversampled frequency* f_s. Furthermore, the quantization noise e_i is introduced at the quantizer level (1-bit ADC).

The signal transfer function $Y(s)$ and the noise transfer function $N(s)$ are then given by equations G.3 and G.4 [7].

$$Y(s) = \frac{H(s)}{1 + H(s)} = \frac{1}{1 + \frac{s}{\omega_p}} \tag{G.3}$$

$$N(s) = \frac{1}{1 + H(s)} = \frac{s}{s + \omega_p} \tag{G.4}$$

Therefore, $Y(s)$ provides low-pass filtering on the input signal while $N(s)$ acts as a high-pass filter for the noise. $N(s)$ provides the so-called *noise-shaping* of the ΔΣ ADC which pushes the noise energy towards the high-frequencies, **out of the desired Nyquist bandwidth**. Thus, the noise-shaping enhances the SNR in the Nyquist bandwidth as the high-frequency region (out of the desired Nyquist bandwidth) is rejected after low-pass filtering (using the digital filter block) and decimation.

Using a *L-order* ΔΣ modulator, it can be shown that a two-times oversampling will lead to an improvement of $L + 0.5$ on the effective number of bits.

For a first-order ΔΣ modulator, a four-times oversampling will lead to a 3-bit improvement while the same oversampling ratio will only lead to a 1-bit improvement for traditional ADCs!

G.3 Digital filter and decimator

As the signal generated by the ΔΣ modulator is binary-encoded, a digital filter can be directly used at the output of the modulator to provide low-pass filtering in order to reject the frequency band outside the desired Nyquist bandwidth. The digital filter also operates at the oversampled frequency f_s and encodes its output on a given number of bits (e.g. 16-bit).

Figure G.3 shows the typical arrangement of a *Finite-Impulse-Response* (FIR) digital filter. Each *Delay* block represent the atom transfer function $A(z) = z^{-1}$ used to construct the low-pass filter transfer function. The output of each delay block is then multiplied by a weight b_i. By adjusting the weights b_i, the desired FIR filter can be formed. All the branches are then added together to form the output signal. Equation G.5 shows the transfer function of the topology shown in figure G.3.

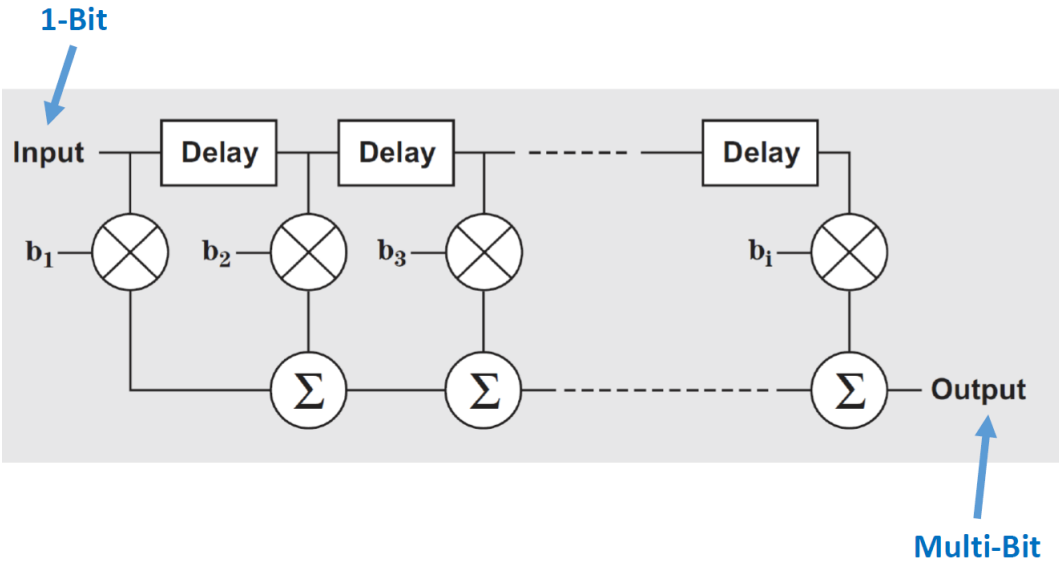


Figure G.3 – Digital filter topology [7].

$$H(z) = \sum_{i=1}^{N} b_i z^{-(i-1)} \tag{G.5}$$

As shown by figure G.3, the output of the digital filter is coded on multiple bits and sampled at the oversampled frequency f_s. A decimator is then used to reduce the sampling frequency to the Nyquist sampling rate f_D as the decimated samples do not convey any additional information according to the Shannon-Nyquist theorem [17].

Figure G.4 shows the effect of the decimation block on the output signal of the digital filter.

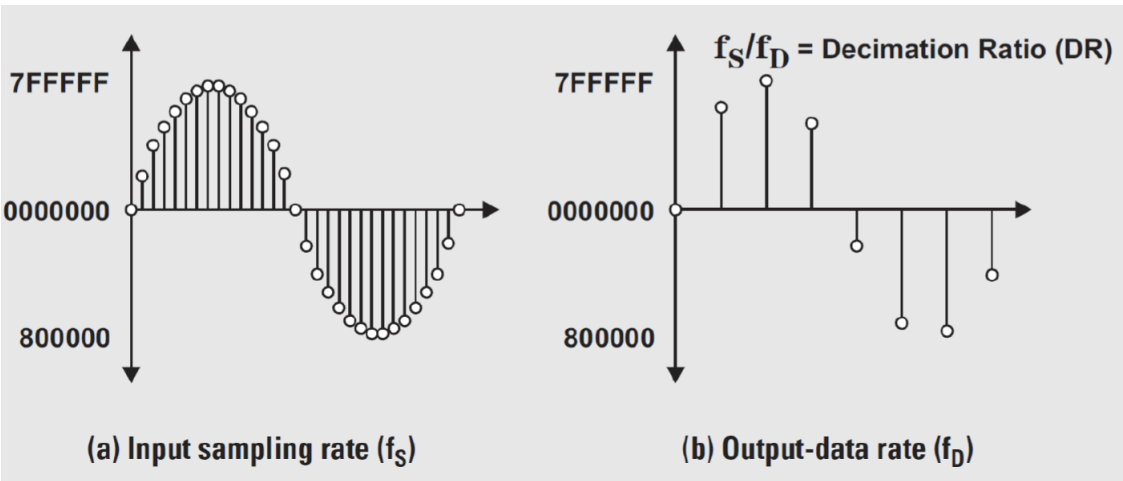


Figure G.4 – Effect of decimation [7].

G.4 Conclusion

In this project, a ΔΣ ADC available in the PSOC has been used as part of the high-voltage regulation loop because of its higher precision (number of effective bits) compared to the SAR ADCs also available in the PSOC. Even if the SAR ADCs were able to reach higher sampling frequencies, the ΔΣ ADC available in the PSOC was able to reach the desired sampling frequency of 10 kHz while having a higher precision, which motivated its use within the high-voltage regulation loop.

Appendix H

TREDI 2020 "Trento" Workshop

TREDI2020: 15th "Trento" Workshop on Advanced Silicon Radiation Detectors

Contribution ID: **17** Type: **contributed talk**

Compact IV/CV measurement instrument for silicon sensors

Wednesday, 19 February 2020 15:40 (20 minutes)

IV and CV curves of are crucial measurements required to characterise silicon sensors. They have to be performed at reception and at several steps of particle detector modules assembly procedure to spot potential damages, at least in the prototyping phase.
High voltage (1kV) biasing of those sensors and accurate, low current measurements (50µA max) are mandatory for this. Typical instruments to perform those measurements are high voltage electrometers and LCR meters with proper decoupling. Those instruments are rather expensive (10k euros range) and commonly have over-specifications for this precise task. We developed a system tailored to perform both IV and CV measurements of sensors in one compact, lower cost instrument. It is based on a PCB that implements a low ripple (100mV) 1kV high voltage power supply, high-side AC/DC current measurement with 15nA granularity. Coupled with an external signal generator and a computer that extracts electrical parameters and IV/CV curves, a Programmable System-On-Chip (PSOC) handles sources control in addition to current, voltage and voltage/current phase measurements. On top of that, temperature, relative humidity are monitored and low voltage DC regulators can supply readout electronics of a fully assembled module to provide a standalone test station usable in sensor/module characterisation or in thermal cycling.

Primary authors: VANLAER, Pascal (Universite Libre de Bruxelles (BE)); DE LENTDECKER, Gilles (Universite Libre de Bruxelles (BE)); ALLARD, Yannick (Universite Libre de Bruxelles (BE)); SAFA, Ali (Universite Libre de Bruxelles (BE)); Prof. ROBERT, Frédéric (Université Libre de Bruxelles)

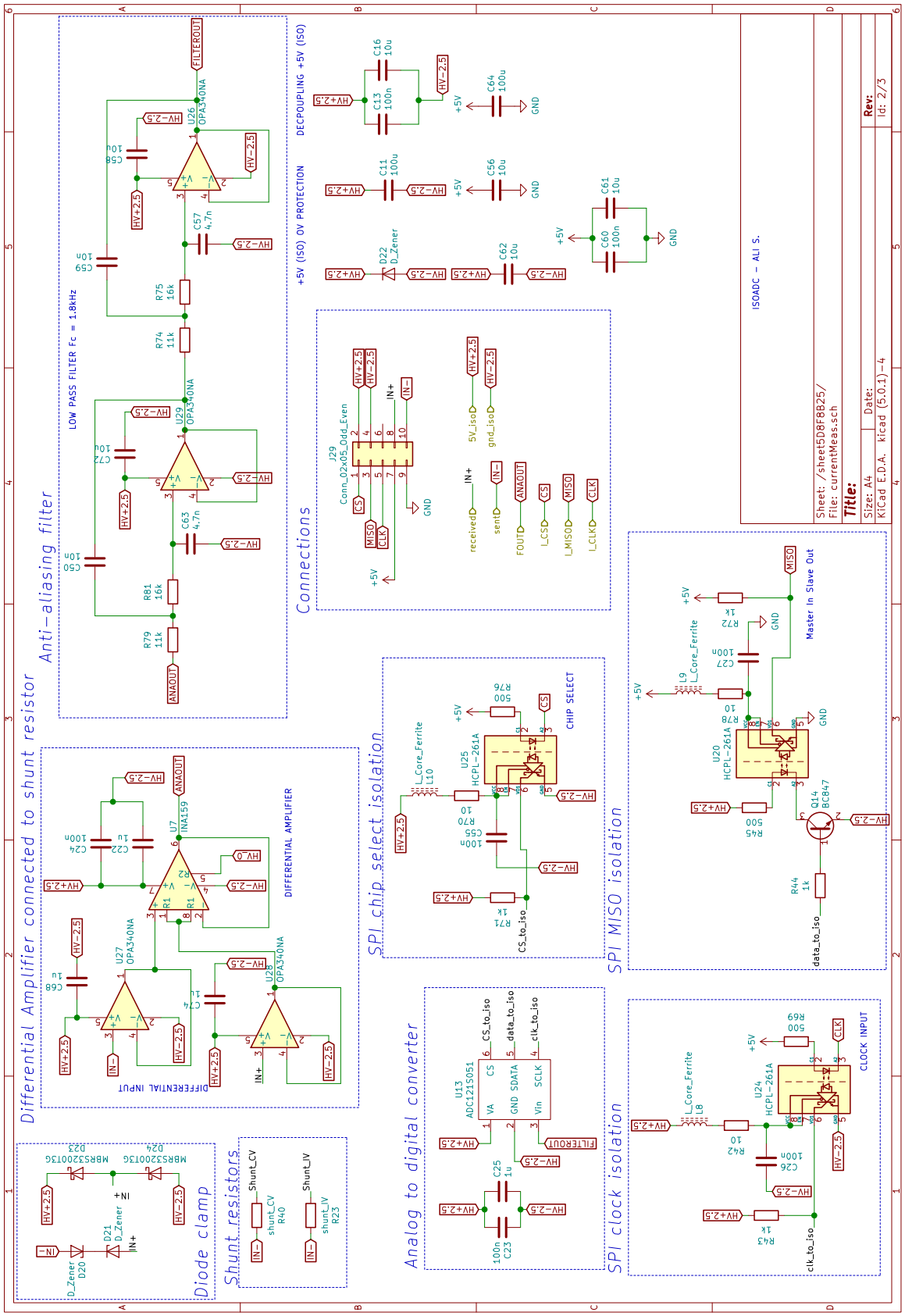
Presenter: SAFA, Ali (Universite Libre de Bruxelles (BE))

Session Classification: Materials, Characterisation, Electronics

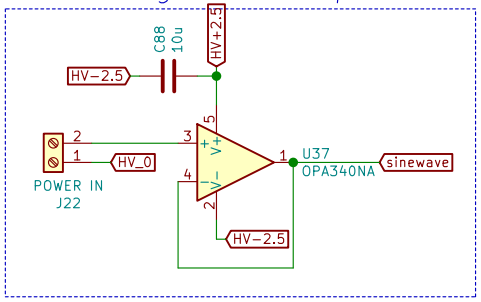
Track Classification: Characterization (TCT and others)

Appendix I

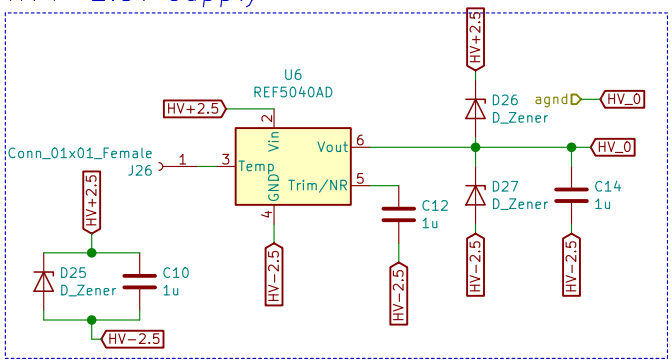
Slow Control Board Schematic



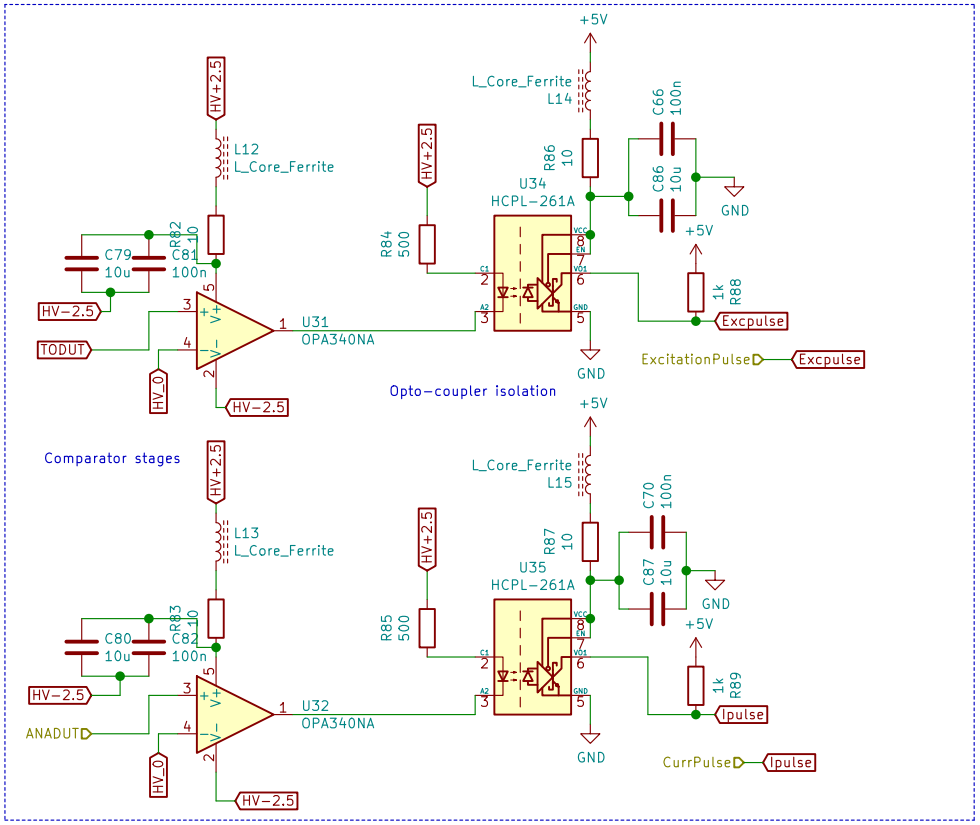
Sine wave generator input buffer



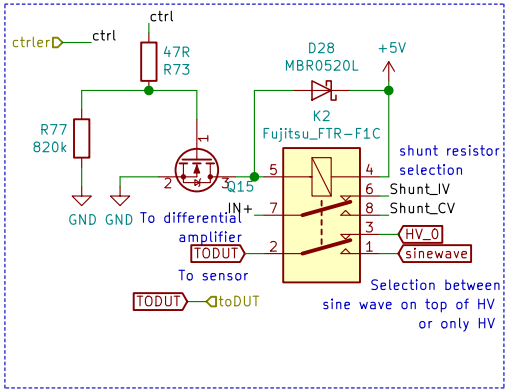
HV+−2.5V supply

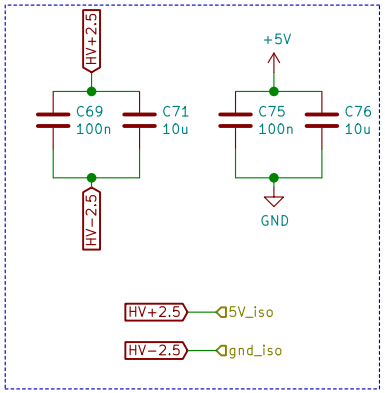


Isolated comparator. Sine to pulse converter



Selection relay between IV and CV modes

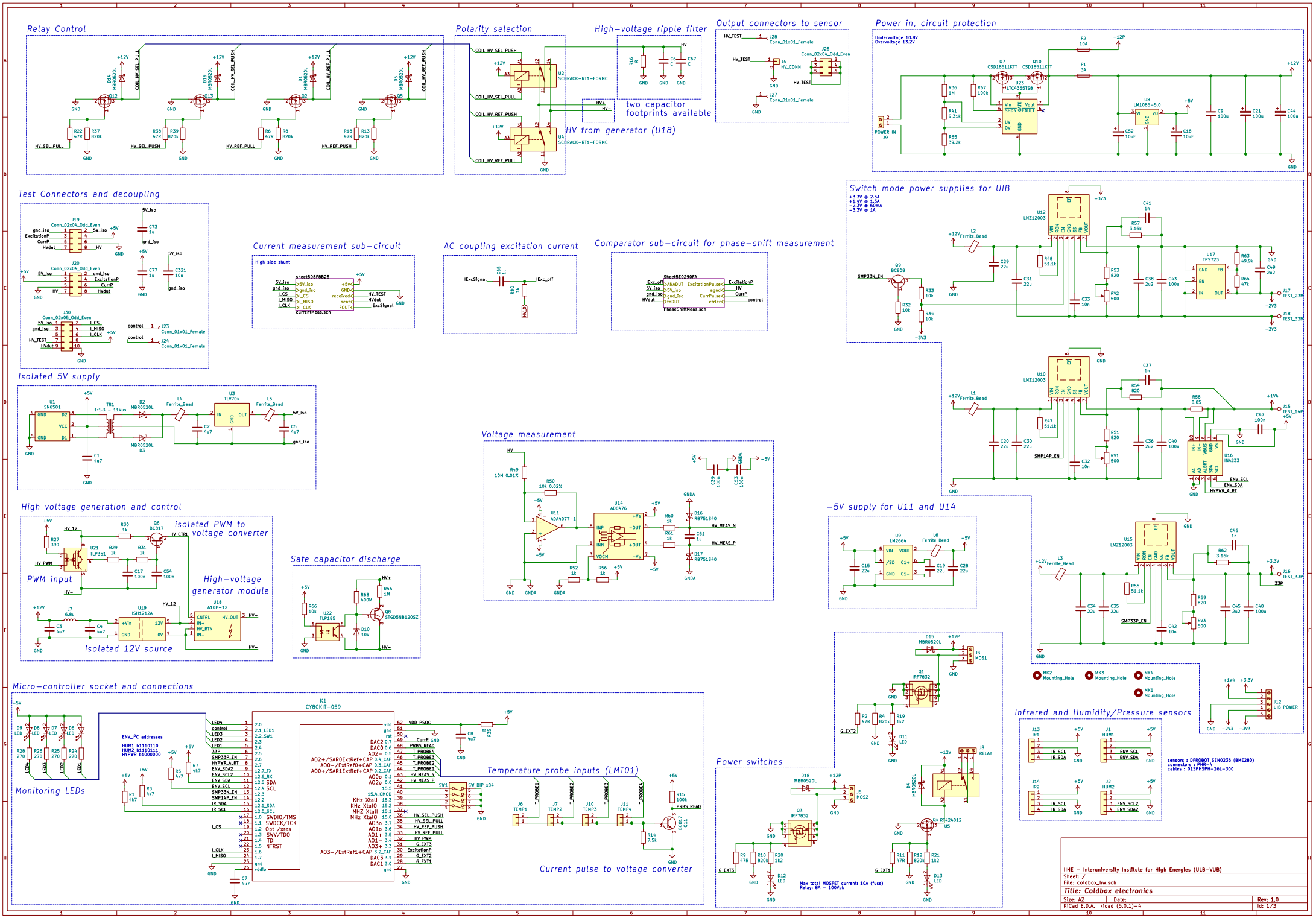




Sheet: /Sheet5E0290FA/
File: PhaseShiftMeas.sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.0.1)−4		Id: 3/3


Relay Control
Polarity selection
High-voltage ripple filter
two capacitor footprints available
HV from generator (U18)
Output connectors to sensor
Power in, circuit protection
Undervoltage 10.8V
Overvoltage 13.2V
Test Connectors and decoupling
Current measurement sub-circuit
High side shunt
currentMeas.sch
AC coupling excitation current
Comparator sub-circuit for phase-shift measurement
PhaseShiftMeas.sch
Switch mode power supplies for UIB
+3.3V @ 2.5A
+1.4V @ 1.5A
-2.3V @ 50mA
-5.3V @ 1A
Isolated 5V supply
Voltage measurement
-5V supply for U11 and U14
High voltage generation and control
isolated PWM to voltage converter
PWM input
High-voltage generator module
isolated 12V source
Safe capacitor discharge
Micro-controller socket and connections
ENV_I²C addresses
HUM1 b1110110
HUM2 b1110111
HYPWR b1000000
Monitoring LEDs
Temperature probe inputs (LMT01)
Current pulse to voltage converter
Power switches
Max total MOSFET current: 10A (fuse)
Relay: 8A - 100Vpk
Infrared and Humidity/Pressure sensors
sensors : DFROBOT SEN0236 (BME280)
connectors : PHR-4
cables : 01SPHSPH-26L-300
IIHE - Interuniversity Institute for High Energies (ULB-VUB)
Sheet: /
File: coldbox_hw.sch
Title: Coldbox electronics
Size: A2
Date:
Rev: 1.0
KiCad E.D.A. kicad (5.0.1)-4
Id: 1/3

Bibliography

[1] Collaboration C. (Date accessed: 30.05.2020) The Phase-2 Upgrade of the CMS Tracker. Geneva: CERN; 2017. CERN-LHCC-2017-009. CMS-TDR-014. Available from: https://cds.cern.ch/record/2272264.

[2] Lenzi T. Development of the DAQ System of Triple-GEM Detectors for the CMS Muon Spectrometer Upgrade at LHC. PhD thesis, Université Libre de Bruxelles; 2016.

[3] Collaboration C. (Date accessed: 4.06.2020) The CMS experiment at the CERN LHC. The Compact Muon Solenoid experiment; 2008. Also published by CERN Geneva in 2010. Available from: https://cds.cern.ch/record/1129810.

[4] Hartmann F. Evolution of Silicon Sensor Technology in Particle Physics. Springer Tracts Mod Phys. 2009;231:1–204.

[5] Vanlaer P. Lectures on Tracking. SPA, Belgium: Belgium-Nederland-Deutschland doctoral school of particle physics; 2019.

[6] (Date accessed: 30.05.2020) Cypress PSOC CY8C58LP Family Datasheet;. Available from: https://www.cypress.com/documentation/datasheets/psoc-5lp-cy8c58lp-family-datasheet-programmable-system-chip-psoc.

[7] Baker B. (Date accessed: 30.05.2020) How delta-sigma ADCs work. Texas Instruments, 2016;. Available from: http://www.ti.com/lit/an/slyt423a/slyt423a.pdf?&ts=1589879555572.

[8] Apollinari G, Béjar Alonso I, Brüning O, Lamont M, Rossi L. (Date accessed: 30.05.2020) High-Luminosity Large Hadron Collider (HL-LHC): Preliminary Design Report. CERN Yellow Reports: Monographs. Geneva: CERN; 2015. Available from: https://cds.cern.ch/record/2116337.

[9] De Lentdecker G, Vanlaer P. Tracking detectors at colliders. 2018, PHYS-F420, Université Libre de Bruxelles;.

[10] Rosa J. (Date accessed: 30.05.2020) Characterizing the VFAT3 chip for the DAQ electronics of the CMS detector; MSc thesis, Université Libre de Bruxelles, 2017. Available from: https://cds.cern.ch/record/2290728.

[11] Maerschalk T. (Date accessed: 30.05.2020) Study of Triple-GEM detector for the upgrade of the CMS muon spectrometer at LHC; 2016. Available from: https://cds.cern.ch/record/2291028.

[12] Neamen D. Semiconductor Physics And Devices. 3rd ed. New York, NY, USA: McGraw-Hill, Inc.; 2003.

[13] Lutz G. (Date accessed: 30.05.2020) Silicon radiation detectors. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors

and Associated Equipment. 1995;367(1):21 – 33. Proceedings of the 7th International Wire Chamber Conference. Available from: http://www.sciencedirect.com/science/article/pii/0168900295007911.

[14] Ravera F. Software Overview Slides. 3rd Tracker Upgrade DAQ school. 2019;.

[15] Sonntag D. Important New Values of the Physical Constants of 1986, Vapour Pressure Formulations based on the IST-90 and Psychrometer Formulae. Z Meteorol. 1990;70(5):340–344.

[16] Durand R. CoolBox board V.1 technical document. Brussels; 2018.

[17] Asch G. Acquisition de données: du capteur à l'ordinateur. Dunod; 2011.

[18] Bourdoux A. Fast DFT Algorithms. technical document, June 2012, imec, Belgium;.

[19] Harris FJ. On the use of windows for harmonic analysis with the discrete Fourier transform. Proceedings of the IEEE. 1978 Jan;66(1):51–83.

[20] Proakis JG, Manolakis DG. Digital Signal Processing (3rd Ed.): Principles, Algorithms, and Applications. Upper Saddle River, NJ, USA: Prentice-Hall, Inc.; 1996.

[21] Brandt A. Noise and vibration analysis: signal analysis and experimental procedures. John Wiley and Sons.; 2011.

[22] James G, Witten D, Hastie T, Tibshirani R. An Introduction to Statistical Learning: With Applications in R. Springer Publishing Company, Incorporated; 2014.

[23] Bergauer T. The Silicon Strip Sensors of the CMS Tracker. PhD thesis slides, TU Wien, Austria: HEPHY; 2011.

[24] Wambacq P. Analog Electronic Circuits. VUB, Belgium: Course notes from ETRO department; 2018.

[25] Lataire J. Measurement Techniques. VUB, Belgium: Course notes from ELEC department; 2018.

[26] Robert F. Théorie des champs. Université Libre de Bruxelles, Belgium: Course notes from BEAMS department; 2018.

[27] Yiu J. The definitive guide to the ARM Cortex-M3 and Cortex-M4 processors. third edition, Elsevier, October 2013;.

ULB UNIVERSITÉ LIBRE DE BRUXELLES

ULB UNIVERSITÉ LIBRE DE BRUXELLES

Exemplaire à apposer sur le mémoire ou travail de fin d'études,
au verso de la première page de couverture.

Réservé au secrétariat :	**Mémoire réussi***	**OUI**
	NON	

CONSULTATION DU MEMOIRE/TRAVAIL DE FIN D'ETUDES

Je soussigné

NOM : Safa

PRENOM : Ali

TITRE du travail : Characterisation of the new tracker sensors for the CMS experiment at CERN.

AUTORISE*

~~**REFUSE***~~

la consultation du présent mémoire/travail de fin d'études par les utilisateurs des bibliothèques de l'Université libre de Bruxelles.

Si la consultation est autorisée, le soussigné concède par la présente à l'Université libre de Bruxelles, pour toute la durée légale de protection de l'œuvre, une licence gratuite et non exclusive de reproduction et de communication au public de son œuvre précisée ci-dessus, sur supports graphiques ou électroniques, afin d'en permettre la consultation par les utilisateurs des bibliothèques de l'ULB et d'autres institutions dans les limites du prêt inter-bibliothèques.

Fait en deux exemplaires, **Bruxelles, le** 4/6/2020

Signature

Formulaire version 04/2015

** Biffer la mention inutile*

** Biffer la mention inutile*

ULB UNIVERSITÉ LIBRE DE BRUXELLES

ULB UNIVERSITÉ LIBRE DE BRUXELLES

Exemplaire destiné à l'étudiant.

Réservé au secrétariat : Mémoire réussi*	**OUI**
NON	

CONSULTATION DU MEMOIRE/TRAVAIL DE FIN D'ETUDES

Je soussigné

NOM : Safa

PRENOM : Ali

TITRE du travail : Characterization of the new tracker sensors for the CMS experiment at CERN.

AUTORISE*

~~**REFUSE***~~

la consultation du présent mémoire/travail de fin d'études par les utilisateurs des bibliothèques de l'Université libre de Bruxelles.

Si la consultation est autorisée, le soussigné concède par la présente à l'Université libre de Bruxelles, pour toute la durée légale de protection de l'œuvre, une licence gratuite et non exclusive de reproduction et de communication au public de son œuvre précisée ci-dessus, sur supports graphiques ou électroniques, afin d'en permettre la consultation par les utilisateurs des bibliothèques de l'ULB et d'autres institutions dans les limites du prêt inter-bibliothèques.

Fait en deux exemplaires, **Bruxelles, le** 4/6/2020

Signature

** Biffer la mention inutile*

** Biffer la mention inutile*

Formulaire version 04/2015